Circuit & Application
Adiabatic logic gates for very low power applications. Process technology used was 180nm

Problem Formulation and Goals
Energy dissipation was increasing dynamic power and leakage current because of the growing number of transistors on a chip. However, the capacity of batteries did not increase in the same way. Energy dissipation of the adiabatic circuits relied on analog properties of the transistors. The design goal was to reduce power and increase robustness and yield.

Step 1 — Nominal Diagnosis
The impact of device W/L ratio on energy dissipation showed different trends for each source of dissipation. Using WiCkeD’s DFM Diagnosis the performance dependency and parameter redundancies were identified and clearly visualized. The designers were able to analyze the link between component values and power dissipation to modify the circuit interactively with WiCkeD.

Step 2— Nominal Optimization
Circuit devices were sized by WiCkeD such that the power dissipation was as low as possible without lowering the frequency. The input signals were shifted by –90°.

Step 3 — Tolerance Analysis and Worst-Case Diagnosis
The Tolerance Analysis measured the influences of the process variation of the circuit. Using this information together with the Worst-Case Diagnosis, designers were able to size the devices to maximize robustness with respect to the process variations.

Step 4 — Monte Carlo Analysis
Monte Carlo analysis validated the expected parametric yield the designers achieved with interactive design centering.

Solution using WiCkeD

WiCkeD Results

Value added of using WiCkeD:
- Power dissipation reduced 50%
- Crossover frequency over 1GHz
- Increased yield to ~97%

Design Problems without WiCkeD:
- High power consumption
- Low robustness
- Low yield (40%)