Reliability-Based Design using MunEDA WiCkeD™

WiCkeD for Reliability-Based Design - User Benefits

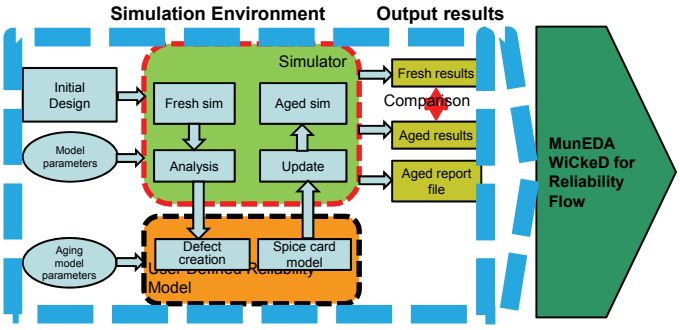
- **Secure chip reliability with accurate device sizing can be now extended across the so-called overdrive designs approach**
- **Consider the main aging mechanisms HCI, BTI and TDDB during circuit sizing**
- **Optimize Performance @ Nominal + Worst Case Operating Conditions & Corners while keeping device stress within reliability margins**
- **Increase design quality minimizing the aging impact on IP area**
- **Automatic design flow to meet tight specifications, improving reliability margin with strongly reduced design time**

Reliability-Based Design Objectives & Challenges

The major challenges for reliability designs revolve around the following topics

- **Increased sensitivity to aging**
  - deep submicron technologies with lower power supply are expected to degrade the performances over time
  - Aging mechanisms are no longer negligible, hence a further degree of complexity has to be taken into account
  - Overdrive design approach requires capturing all aging instances with high accuracy, efficiency and scalability in a fully automated way
  - cascoded architectures are no longer enough to keep aging mechanisms within the "safe region"
- **Achieve circuit robustness in the presence of transistor aging as follows**
  - Performance optimization both for fresh and aged designs with reliability constraints to detect the device extra stress during signal transition
  - Suitable device reliability scaling models to accurately measure the device stress during simulation in static and transient conditions
- **Powerful design methodology to increase circuit reliability and designer confidence**
  - Size the circuit for fresh and aged designs, while keeping the device degradation below the overall reliability margins
  - Capability to deal with device degradation at early design stage to quickly highlight circuit weakness
  - Multi test-benches are required to address all design specifications before and after aging mechanisms

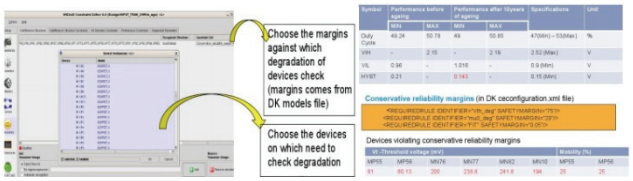
Solution – MunEDA WiCkeD Simulation & Sizing Flow with Aging



The future CMOS designs are moving towards topologies working at higher frequencies and operating in harsh environments, under constraints of reduced area and low power consumption. Furthermore, the usage of constant voltage scaling scheme to achieve higher performance benefits by the overdrive approach, increasing the devices' stress. In this context cascoded CMOS architectures are no longer enough, they require the strong need to benchmark products for their end-of-life performances with higher accuracy. Moreover, it is key to capture the aging effect of all instances during design and not as final check before moving to layout. Indeed, in IOs drivers, mixed-voltage I/O interfaces, it is common during transition, that MOSFETS get stressed because of the "different" time-constants of their drain and source nodes. Even though the circuit meets all the DC and transient specifications it is not reliable.
Therefore, the reliability effects must be treated as a time-evolving variability in order to gain a firm understanding of the mechanisms leading to device degradation and their impact on circuit and system performance.
It becomes important to rely on a design environment wherein aging mechanisms are calculated over the life-time, extracted in a report file so that software capabilities can then use the results to achieve the required level of reliability and robustness.
Circuit analysis and sizing can be performed using different analysis and optimization tools of MunEDA WiCkeD to overcome the new challenges designers are faced with.

The analysis and optimization flow start with the circuit setup, using the powerful WiCkeD Constraint Editor (CED) to load all the main features (topology, performances, technology), with the pre-defined reliability and DC operating constraints.

WiCkeD Reliability Constraints Setup and Simulation Results



The user can automatically exploit the area feature to limit the total area below a maximum value. This will accomplish one of the main key points that is the trade-off between reliability and area.
Using WiCkeD WCO Worst Case Operation user can quickly cross-check the worst case performances against operating parameters. Moreover, using the WiCkeD BAS Basic & Sensitivity Analysis, user can identify and quantify the relative influence of each design and operating parameter against performances and constraints. This will offer a better insight into possible circuit limitations. The parameter sweep can be run on the most influent parameters to detect possible performance non-linearities against parameters.
After circuit analysis, with WiCkeD FEA Feasibility Analysis it is possible to change the values of design parameters in a way that both DC operating constraints (namely structural constraints) and reliability constraints are fulfilled with nominal and worst case operating conditions. Consequentially, the circuit will work in the technically correct and reliable region at the same time.
Users can now start the powerful and numerous silicon-proven optimization algorithms of WiCkeD DNO Deterministic Optimization to improve the performance values in typical and worst case operating condition by changing design parameter values with a unique gradient-based optimization algorithm. Whereas with FEA, only constraints are fulfilled for robustness and reliability purposes, DNO improves all the performances keeping the circuit in the feasibility region. This ensures at the end of the flow, a circuit which meets all the specifications in typical and worst case operating conditions, maximizing robustness and reliability as a whole.

MunEDA WiCkeD Analysis and Optimization Reliability Flow

Design Flow	Flow Details	Used Tools
Testcase Selection & Setup	• Main circuit features • Design and operating parameters • performances	Design Framework, Schematic Entry, Simula… Kit
Constraint Editor Setup	• Circuit parameterization • Load DC operating constraints • Load reliability constraints	CED
Worst Case Operation & Corners Values	• Cross check performance with worst case operating conditions and corners	WCO
Sensitivity Analysis and Parameter Sweep	• Detect parameter relative influence • Check for high order non-linearities	BAS

Feasibility Optimization	• Gradient based optimization to
	  • Fulfil structural constraints
	  • Fulfil reliability constraints
	  • Achieve robustness and reliability
		FEA

Nominal Optimization at typical operating conditions	• Gradient based optimization to
	  • Meet specification @nominal and while considering structural and reliability constraints as a whole
	  • Find a good starting point for next step
		DNO

Nominal Optimization including all Worst Case Operating ondition	• Gradient based optimization to • Meet specification @nominal and Worst Case Operating conditions while considering structural and reliability constraints as a whole	DNO
Results: reliability & robustness achieved!	• Achieve performances specification • Fulfil structural and reliability constraints • No stress violation before going to layout	

MunEDA WiCkeD – Technology Support & Results

- **WiCkeD is integrated and supports the major design frameworks and SPICE/FASTSPICE/RF simulators as well as stand-along or customized environment/s**
- **MunEDA WiCkeD supports many different foundry technologies and PDKs in different nodes**
- **Ensure to meet tight specifications and widen design reliability margins**
- **improve designer efficiency to achieve a significant design time reduction**
- **Reliability based design optimizations can be extended for overdrive designs**

Reference: STMicroelectronics – Design Optimization in Deep-submicron technologies covering methodology for reliability based circuit optimization for IOs – MUGM MunEDA User Group Meeting 2013