MunEDA

High Sigma Yield & Robustness Analysis and Optimization

High Sigma Yield Analysis & Optimization with MunEDA WiCkeD

WiCkeD High Sigma Analysis and Optimization - Highlights

- **Fast, efficient, cost effective**
- **Robust & Standard Yield Estimation**
- **High-Sigma Yield & Robustness Estimation**
- **Sampling-based and Deterministic Yield Analysis Methods**
- **Saves on unnecessary silicon runs**

Circuit Application examples

- Memory (SRAM, DRAM, CRAM, Flash, Embedded, FPGA, etc.) – Sense Amplifier, Bit Cells, Memory Interfaces
- Standard Cells, Flip Flop, Multibit Register, Look-up Tables
- Comparator, ADC, Transceiver, Bandgap, Charge Pump
- PLL, VCO, Oscillator, Filter, OpAmp, SerDes
- … and many more

Challenges for high-sigma circuits and designs

Yield estimation, optimization and verification for high-yielding circuits such as SRAM or CRAM requiring high-sigma robustness is very challenging compared to other circuits:

- Such cells often appear by **thousands or even millions on one chip**
- The failure of any individual cell can result in the **failure of the entire systems** or chip, if no redundancy is implemented

For these cells it is critical to design cells with **extremely low failure probability**

- Typically a yield estimation method must be able to predict yield higher than 0.9999 → at the tail of the distribution (>6σ for a Gaussian distribution) especially if some circuit performances (e.g. write time) show non-Gaussian distributions with long tails

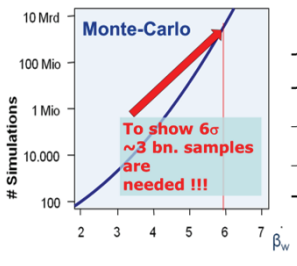
High-Sigma Estimation in WiCkeD – Monte Carlo Analysis

MunEDA WiCkeD includes several Monte Carlo Methods like

- **Direct Monte Carlo (DMC)**
- **Quasi-Monte Carlo (QMC)**
- **Important Sampling (IS)**

Monte Carlo is seen as **established and very robust yield estimation method**, nevertheless all Monte Carlo Methods are limited and **can not handle** efficiently ultra high-sigma (>6σ) robustness analysis and not even **circuit optimization tasks**. Like also described in the figures below the verification of a yield Y > Y_{min} with 95% confidence for counting Method DMC is because of the huge required simulation number not feasible or realistic.

Conventional Monte Carlo	WiCkeD MCA Monte Carlo Analysis
Run MCA at all corners	+++ (optional) dynamic calculation of worst-case operating conditions to save simulation runs
Distribute only complete batch	+++ Truly distributed simulations for larger circuits
Only user-defined specs	+++ Specs + structural constraints
Only selected simulators and simulation types	+++ Supports many simulators (e.g. Hsim, XA) and simulation types (e.g. pss-sweep)
No correlation between testbenches	+++ Define "Physical Identical Devices" to calculate correct correlation between testbenches
Limited or no graphical analysis	+++ Interactive scatter plots, advanced sensitivities, outlier removal, …



$N > 3 / (1 - Y_{min})$

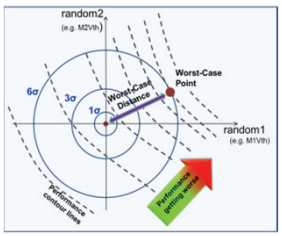
Y_{min}	$1-Y_{min}$	β_w	N
98%	2%	2σ	150
99.9%	0.1%	3σ	3 000
99.997%	0.003%	4σ	100 000

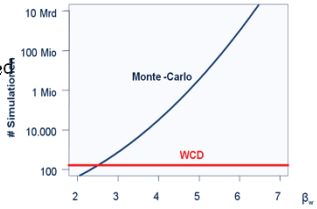
High-Sigma Estimation in WiCkeD – Worst Case Analysis

The Worst Case Analysis methods in WiCkeD are based on the calculation of the Worst-Case Point (WCP) and **Worst-Case-Distances (WCD)**. This is the point on the specification boundary closest to the mean value. In WiCkeD WCP/WCD are calculated for every parameter simultaneously to verify consistent designs.

WiCkeD **W**orst-**C**ase **A**nalysis (**WCA**)

- finds the combination of process parameter values that is most likely to violate the spec → base for Yield Analysis
- WCA is efficient and can handle non-Gaussian specs with long tails
- The effort grows only linearly with the number of process parameters
- **Can handle >6 sigma** and higher robustness measures easily
- Needs much fewer samples compared to Monte Carlo Methods
- WCA/WCD results **can be used** efficiently **for Robustness & Yield Optimization**





High-Sigma Estimation in WiCkeD – Sensitivity Analysis

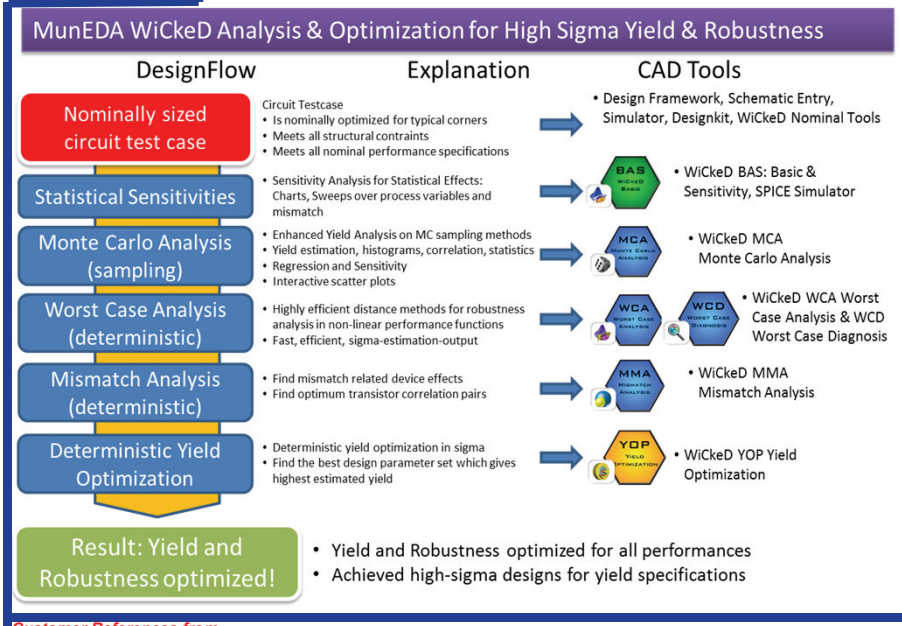
With WiCkeD BAS Sensitivity Analysis Designers can do **sensitivity calculation** (e.g. geometries, process, operating conditions, mismatch) and **sweeps** for all kinds of analyses (DC, AC, Tran, RF, …) using all kind of industrial SPICE/FastSPICE simulators. The sweeps include constraint violation markers to verify designs will not be violated.

High-Sigma Estimation in WiCkeD – Mismatch Analysis

The WiCkeD deterministic mismatch analysis MMA **identifies and analyses mismatch-relevant transistor pairs** on selected circuit performances. The variance of these local variations will be analyzed based on dependencies of device pair geometries.

MunEDA WiCkeD – Technology Support

- WiCkeD is integrated and supports the major design frameworks and SPICE & FastSPICE simulators and simulation environments
- MunEDA WiCkeD supports many different foundry technologies and PDKs in many different technology nodes
- For more information and support contact www.muneda.com



Customer References from MunEDA User Group:

- **Samsung:** High-speed memory interface WCA design in 14nm FinFET (MUGM 2013)
- **SKHynix:** 1300 Transistor Receiver for DRAM Cells in 28nm (MTF Korea 2013)
- **Altera:** 6,5σ High-Sigma Memory Cell WCA for FPGA in 40nm (MUGM 2010)
- **STMicroelectronics:** 200k-Devices High-Speed Clock Generator MCA in 65nm (2012)