Automated Design Migration & IP Porting Flow for Custom Circuits

Automated Design Migration & Porting Flow - User Benefits

- Customer proven and automated flow for Design Migration & IP Porting of existing IP between different process technologies
- Fast Schematic Migration with MunEDA SPT Schematic Porting Tool
- Efficient Re-Sizing with MunEDA WiCkeD Analysis and Sizing Tools
- Save Time and Efforts
- Make designer's life more convenient and results reliable

## Design Migration and Porting between Different Processes

With the trend to go fabless, many chip designs have to be migrated between process technologies and within internal and external foundry processes. MunEDA tools solve the challenges of such difficult design migration & sizing for full-custom designs.

At the beginning of – or during – a new design project, it is often necessary to use and re-use available IP (intellectual property) and circuits from previous projects, instead of designing everything from scratch. Often a new design uses a new or different process technology. Thus, it is necessary to migrate and apply given circuit IP for use with this new target technology. Consequently, circuit designers must adapt circuits to the new process by a time-consuming and tedious manual process very often .

Overview – Circuit & IP Porting and Re-Sizing Flow

Circuit & IP Migration and Porting usually follows a structured 2-step design flow. In the first phase the given schematics and topologies will be converted from the source to the target technology. In the second phase this circuits and IP will be sized for the new target specifications and optimized for the new target process technology.

Full Custom Circuit Design Migration Flow
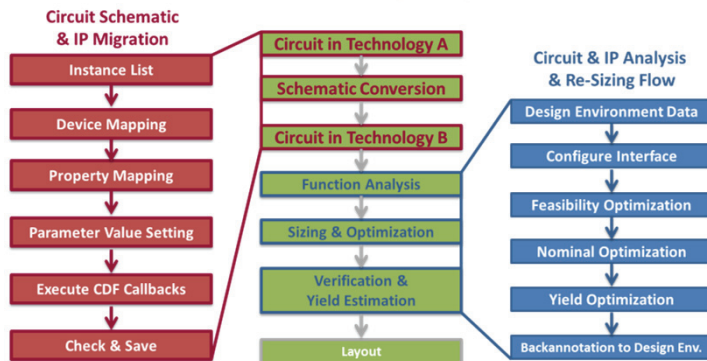
Design Migration & IP Porting – Types and Challenges

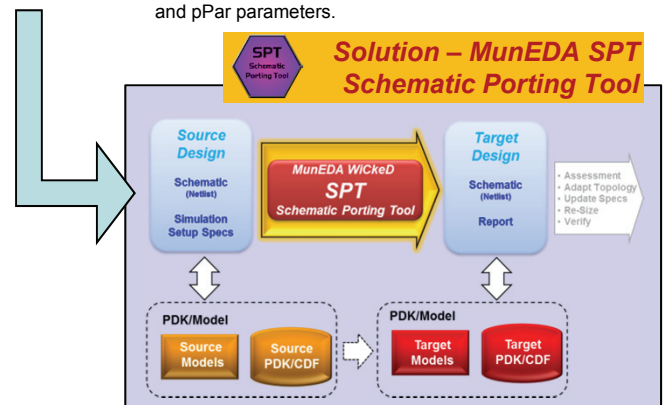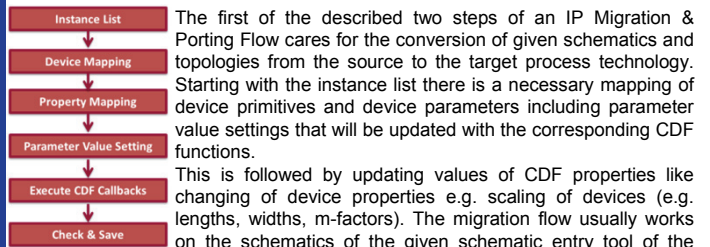Design migration & IP porting can be versatile, and it includes different tasks:
- **Horizontal Porting:** Migrating IP from one technology node to the same node of a different foundry due to foundry migration, second sourcing or fab consolidation.
- **Vertical Porting:** Migrating IP from a technology node to a smaller one, usually from the same fab or foundry.

Both are challenging, especially for analog-/mixed-signal designs, RF designs, IP libraries and memory cells because many blocks and even entire SoCs must be migrated in a short time, mostly by a very limited number of designers. Furthermore, there is no simple rule for shrinking AMS/RF, I/O and full-custom digital designs. Every block needs adjustment of geometries, biasing, etc. even if specs don't change. Therefore, it is necessary to migrate and port the schematics individually to conform with technology constraints, or to meet enhanced functionality or performance specifications.
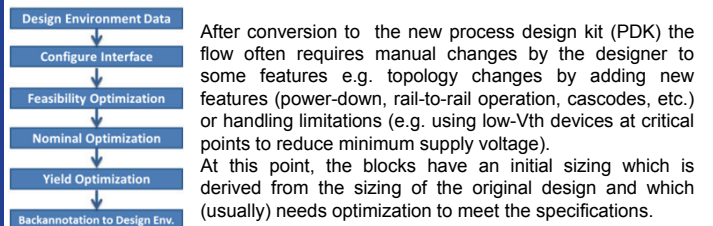
Migrating IP is a challenge because:
- Different device parameters (vth, etc.) require adjustment of biasing and small-signal parameters
- W, L shrinking is desirable, but not as simple as digital
- Some devices (mimcaps, inductors, etc.) may or may not be available, or may be of a quite different type
- Circuit topology may need modification
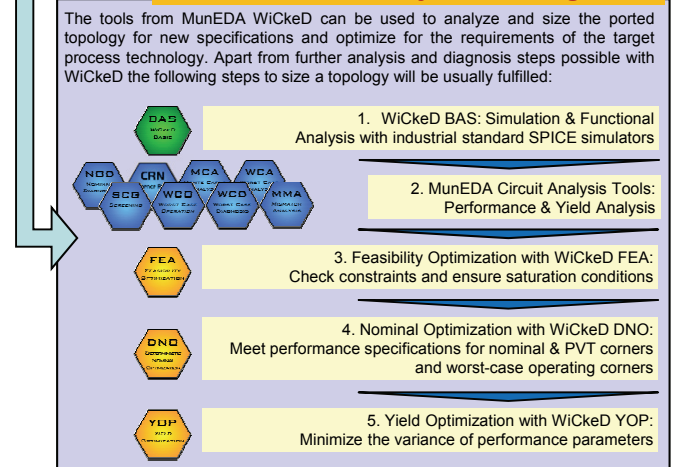- Layout shrinking in integrated technologies is insufficient

Step 1 – Automated circuit schematic migration from source to new target process technology

The first of the described two steps of an IP Migration & Porting Flow cares for the conversion of given schematics and topologies from the source to the target process technology. Starting with the instance list there is a necessary mapping of device primitives and device parameters including parameter value settings that will be updated with the corresponding CDF functions.

This is followed by updating values of CDF properties like changing of device properties e.g. scaling of devices (e.g. lengths, widths, m-factors). The migration flow usually works on the schematics of the given schematic entry tool of the used design environment and is supporting design variables and pPar parameters.

Solution – MunEDA SPT Schematic Porting Tool

Step 2 – Migrated IP Analysis & Re-Sizing Flow

After conversion to the new process design kit (PDK) the flow often requires manual changes by the designer to some features e.g. topology changes by adding new features (power-down, rail-to-rail operation, cascodes, etc.) or handling limitations (e.g. using low-Vth devices at critical points to reduce minimum supply voltage).

At this point, the blocks have an initial sizing which is derived from the sizing of the original design and which (usually) needs optimization to meet the specifications.

Solution – MunEDA WiCkeD Circuit Analysis & Sizing Tools

The tools from MunEDA WiCkeD can be used to analyze and size the ported topology for new specifications and optimize for the requirements of the target process technology. Apart from further analysis and diagnosis steps possible with WiCkeD the following steps to size a topology will be usually fulfilled:

1. WiCkeD BAS: Simulation & Functional Analysis with industrial standard SPICE simulators
2. MunEDA Circuit Analysis Tools: Performance & Yield Analysis
3. Feasibility Optimization with WiCkeD FEA: Check constraints and ensure saturation conditions
4. Nominal Optimization with WiCkeD DNO: Meet performance specifications for nominal & PVT corners and worst-case operating corners
5. Yield Optimization with WiCkeD YOP: Minimize the variance of performance parameters

IP Porting with MunEDA Tools – Technology Support

- WiCkeD™ & SPT Design Tool Suites
- Integrated into standard design environments
- http://www.muneda.com/Products
- For more support contact www.muneda.com