Memory Design using MunEDA WiCkeD^{TM}

SRAM – DRAM – Flash – FPGA

WiCkeD for Memory Cell Design - User Benefits

- **Applicable for all kind of memory design (SRAM, DRAM, Flash, FPGA, …)**
- **Analysis of process variations and high-sigma verification**
- **Memory cell & interface optimization with automated sizing and yield optimization**
- **10-100x faster and more efficient than pure manual design**

Challenges in Memory Design

Many building blocks of memory (SRAM, DRAM, Flash, FPGA) are very sensitive to process variation, supply voltage, leakage and mismatch. Top challenge for memory designers are therefore to analyze and optimize the circuit robustness at high levels beyond six sigma, for memory circuits that are sensitive to process variation, supply voltage, leakage and mismatch.

Typical Circuits for memory design are therefore memory cells (bit cells), sense amplifiers, charge pumps, oscillators, receiver paths, decoders, timers, bandgap references, multiplexers and other circuits.

Typical performance metrics for memory designs are e.g. write time, static noise margin, leakage current, power consumption, glitch, offset, accuracy, delays, pin-to-pin-skew and many more.

Challenges in Memory Design – SRAM, CRAM

SRAM & CRAM bit cells require high sigma robustness for local variation (OCV) because they are instantiated in large numbers on a chip on the die, the impact of random local variation must be analyzed to a high sigma level. Large SRAM arrays require robustness levels of 6.5 sigma and higher.

Monte Carlo needs a too large sample size for such high sigma levels due to the long tail distributions of key metrics. To determine the failure rate in the order of one part-per-billion (6 sigma) with 10% error, the sample size has to exceed 380 billion runs what is not realistic to achieve with Monte Carlo based methods.

MunEDA WiCkeD delivers highly efficient methods for bit cell analysis & optimization.

Challenges in Memory Design - DRAM

DRAM designs are highly influenced on short time process changes in the fab. Therefore the fast analysis of existing DRAM chips and underlying circuits is key for successful yield enhancement already in design. As mainly influenced by process variation timing and power are key influence factors for DRAM designs and interfaces. For this reason it is important to design the cells and sensing circuits in a way that it is as much insensitive against the process variations as possible. For this reason highly efficient sensitivity & yield analysis and optimization methods are required.
MunEDA WiCkeD delivers highly efficient methods for analysis & optimization of memory interfaces and sensing circuits.

Challenges in Memory Design - Flash

Flash is a non-volatile memory that is widely used in USB, microSD, SSD, mobile memory, IP3, navigation, digital devices and many more. Based on technology progress flash memory is underlying a constant cell size reduction based on process and design shrink. The reduced margin between the cell distributions lead often to an increased read error rate. Therefore the analysis and optimization of the variation and sensitivity of the read sense amps is very important for good performing and high-yielding flash memory.
MunEDA WiCkeD delivers highly efficient methods for design shrink, analysis & optimization of flash memory.

Challenges in Memory Design – FPGA

FPGA designs are highly dominated by leading-edge process technology and therfore face an agressive development schedule. FPGAs consist of ultra-high density of meanwhile up to billions of transistors or core cells (e.g. CRAM) within the FPGA core with additional transceivers, PCIe hard IP and general-purpose highspeed IOs. For this reason a very specific sigma-variation-stability is required to avoid both underesign that cost yield loss and also expensive overdesign. For FPGA designs therefore methods like sensitivity analyis and worst case analysis are key for core cell design to detect the influence of static noise or mismatch. The interface designs (transceivers, high-speed IOs) and LUT (look-up tables) require highly efficient performance and yield optimization methods to reduce area and keep the delays under control.
Both are included in MunEDA WiCkeD tool suite and proven with FPGA developers worldwide since years.

Testimonial - Seunghwan Lee, Senior Research Engineer, Design Automation Team at SKHynix: "As historically used process corners are too pessimistic and not realistic for todays designs, MunEDAs deterministic circuit analysis and optimization helps us to speed up the design process and to avoid unwanted redesigns."

MunEDA WiCkeD tools for memory cell (bit cell) high-sigma parametric yield verification (SRAM, CRAM)

MunEDA's advanced worst-case analysis (WCA) methodology is the most efficient way to let the user determine realistic and accurate high sigma worst-case conditions of margins, leakage, write times and other metrics. Realistic worst-case bit cell net lists enable failure rate estimation of whole columns and arrays. Particularly for problems with non-linearly bounded failure regions, MOS model discontinuities or multiple failure regions, adaptive WCA tools are more reliable and accurate than choosing sample points by one global response surface model. To compare results, response surface models and importance sampling are available for WiCkeD.

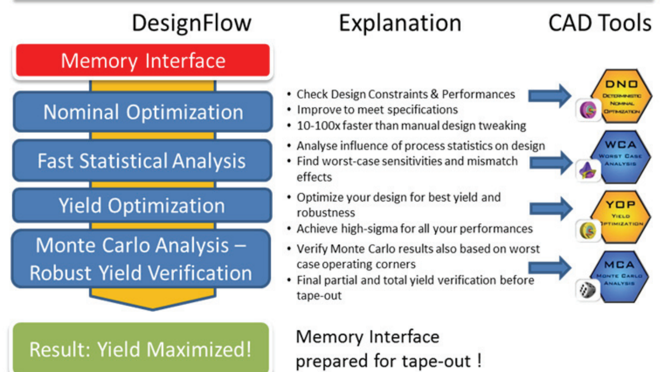
WiCkeD Wost Case Analysis
- Runs 10-100 times faster than Monte Carlo methods
- Yield as sigma calculation from worst case distance

WiCkeD Worst Case Diagnosis
- Understand Performance Variation through Parameter Variation
- Samples in sigma ellipses, Yield calculation

WiCkeD Monte Carlo Analysis
- Enhanced Monte-Carlo Methods for Worst-Case operation corners & Robust Yield Verification
- Verify design limits vs manufacturing process

MunEDA WiCkeD Tools for Memory Interface Development

Designing and verifying high-speed low power memory interfaces such as LPDDR is a challenge for full custom designers. MunEDA WiCkeD provides advanced statistical analysis methods and optimization software to tune I/O circuits for low jitter, duty cycle, low power, reliability and parametric robustness.



MunEDA WiCkeD delivers numerous highly efficient tools for design migration, analysis, and sizing of memory cells and memory interfaces. All tools are proven within the last 10+ years in tape-out and silicon by the leading memory making companies worldwide (See also references below).

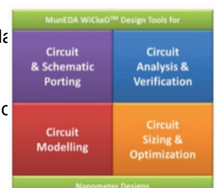
MunEDA WiCkeD fills the functionality gap in existing design frameworks and simulators especially in the memory design area.

Customer References from MUGM MunEDA User Group Meetings:

- ***Altera - Applications of WiCkeD in FPGA Cell Design (MUGM 2010)***
- ***SKHynix - Using WiCkeD in DRAM Development (MUGM 2011)***
- ***Infineon - 6T for Embedded SRAM - six sigma design with WiCkeD (MUGM 2006)***
- ***Microsemi - Using WiCkeD for SRAM sense amp optimization (MUGM 2012)***
- ***STMicroelectronics - Optimization and Centering of the Basic Cells of SRAM Memories with WiCkeD (MUGM 2007)***

MunEDA WiCkeD – General & Tool Support

- WiCkeD is integrated and supports the major design frameworks and analog/RF SPICE & FastSPICE simula as well as stand-along or customized environments
- MunEDA WiCkeD supports many different foundry technologies and PDKs in many different technology nc
- For more information & support: www.muneda.com



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