New Technology Migration Methodology for Analog IC Design

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***Abstract*—In this paper, a new approach for technology migration of full custom IC designs is presented. Differently from previous methodologies, in which the generation of the circuit on the target process is either done manually or at netlist level, the migration is performed on a schematic level, followed by a robustness verification with the usage of MunEDA tools. The methodology is validated and simulation results are presented for the migration of a bandgap voltage reference between two processes of the same technology node, 180μm/1.8V.**

I. Introduction

On the turn of the century, system on chips (SoC) have become a common reality due to shrink of circuit features and increase on transistor density. Those SoCs often contain analog, RF and mixed-signal designs to satisfy the growing demand of communication applications [1]. Meanwhile, time to market requirements of such SoCs must be reduced too, in order to reduce costs. In this context, the reuse of previous designed circuit blocks or available third party Intellectual Property (IP) blocks, becomes of extreme importance.

One aspect of the circuits reuse is the design porting between different CMOS process technologies, which may be a time-consuming and challenging task in a full custom IC design, either for same technology node or different ones. In terms of digital design, reuse of circuits is considerably advanced on system level (ESL) or register-transfer level (RTL) and the reuse of IPs specifically has already been established, reducing design time drastically [2]. However, for analog design, the industry of IPs has not expanded likewise, due to multiple trade-offs that have to be considered on analog circuits, such as gain, noise, power consumption, etc. These specifications are impacted by the manufacturing process. Therefore the reuse of a design in one technology requires analysis and re-sizing to achieve good performance in the new technology, even though specifications and schematics have not changed.

Thus, porting an AMS/RF circuits is time consuming and error-prone and requires the same sizing as a new design to reach reliable performances reliably. Every block must pass through re-design with geometries and bias adjusted. Most design steps are performed manually because there is no simple shrinking rule or factor for AMS or RF integrated circuits as in digital cells. The level of complexity increases as we migrate to smaller technology processes, with changes on power supply and threshold voltage levels that may imply in circuit topology changes also.

Several methodologies and approaches for the analog block reuse can be found, [3]–[11]. References [4], [5] propose a resizing methodology on which the initial scaling is based on level-1 MOS transistor model. The approach on [6] is an analytical resizing based on the Unified Current Control Model [12], UICM, and some experimental results have been explored in [7], and refined in [8], [9]. The methodology shown [10], [11] includes automatic generation of the target netlist. In particular, on [11] circuit reliability and robustness are also considered using extracted layout parasitics.

In general, most solutions propose a division of the porting process in two steps: initial resizing and circuit optimization. The generation of the circuit on the target PDK models, from the original design, is usually done manually, or automatically only at netlist level.

This paper presents a technology migration solution that allows an automatic porting from source to target PDK at schematic level, with user-defined initial resizing followed by robustness verification, with the use of MunEDA Schematic Porting Tool and MunEDA WiCkeD^{TM} Design Tools [13]. Although not covered in this paper, the automatic optimization in the WiCkeD tool suite can be applied beyond porting to achieve better performances in the ported design than the original.

The proposed porting methodology is presented in Section II, as well as an overview of MunEDA tools. A Bandgap Voltage Reference is used as study case. Simulation results are shown in Section III, to validate the proposed approach. In Section IV, time effort for this methodology is discussed. Finally, a conclusion is given in Section V.

II. Proposed Methodology

Porting designs between process technologies efficiently and correctly is a key challenge in full-custom IC design reuse. The porting process can be classified into two types: horizontal and vertical porting. The first corresponds to the migration of designs from one technology node to the same node of a different foundry; in the second, circuit migration is performed from a technology node to a smaller one, usually of the same foundry [14].

MunEDA GmbH proposes a flow solution, shown in Fig. 1 that supports both, horizontal and vertical porting. The solution is divided in three major steps:

1) *Schematic Porting or IP Reuse:* Corresponds to the automated schematic migration between source and tar-

get PDK. This step is done with MunEDA Schematic Porting Tool (SPT).

2) *Design Assessment:* Consists of a first analysis of the migrated circuit to check if the functionality can be achieved with the original topology or making changes if necessary. For horizontal porting it is often sufficient to run a verification, while vertical porting often implies modification of bias and possibly of power supply and subsequently changes on the circuit topology. Such topological changes are done manually by the designer.
3) *Sizing and Sign-off:* Corresponds to the circuit resizing to re-achieve and ensure circuit functionality, performance, yield and robustness in the new process, or beyond porting achieving better performance leveraging benefits of the new process. Performance and robustness can then be documented by running the verification flow. This sizing and verification step is done with MunEDA WiCkeD tool suite.

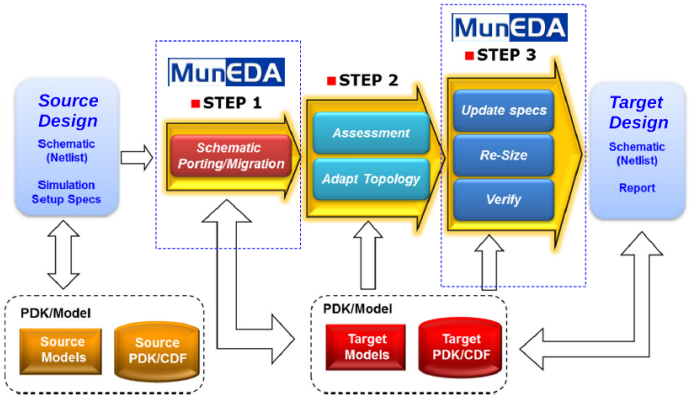

Fig. 1. MunEDA's solution flow [13].

A. Schematic Porting Tool

MunEDA SPT, a commercially available tool, migrates schematics fast and fully automated. During porting, devices from the source PDK are replaced by their counterparts in the target PDK at schematic level and target cell properties are set according to rules defined by the designer. SPT can draw and remove wires, rotate and mirror symbols and also stretch schematics, in case symbols between source and target PDKs differ in size. SPT is fully integrated into the Cadence® Virtuoso® custom design platform.SPT's flow is shown in Fig. 2.

In order to perform migration, a SKILL® file that contains information of both source and target PDK cells, as well as mapping rules regarding property cells and symbols, is needed. Once this conversion rules file exists, porting of a whole library can be done in a matter of minutes.

The conversion rules file is generated from five other files:

- **Cell Mapping Table:** The correspondence between source and target PDK cells is made in this table. Additionally there should be a property and a symbol mapping rule name for each pair.

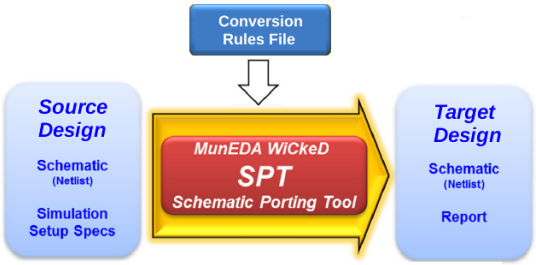

Fig. 2. Schematic Porting Tool flow [13].

- **Property Mapping Table:** This spreadsheet contains the expressions for recalculation of properties of target cells informed on the previous file. For instance, a formula that performs transistor shrinking should be informed here.
- **Symbol Mapping Table:** All symbol transformation between source and target cell, be it rotation, shift or mirror, is informed in this table. Furthermore, if terminal mapping is also needed, due to differences in names or positions, the user should also inform it here.
- **Source CDF:** The CDF dump of the source PDK, generated on Virtuoso.
- **Skill Header File:** On this file, the target library initialization is performed. Additional procedures, that are executed prior and after the migration, may also be defined on this file. Those procedures allow SPT to add a global net to a dangling pin, or assign a value to a substrate node defined as property, among others.

B. WiCkeD Tool Suite

The WiCkeD tool suite provides a methodology solution for full-custom circuit analysis and optimization. In WiCkeD, device geometries of transistors and passive devices are assumed as design parameters. The circuit working conditions such as temperature, voltage supply or load are treated as operating parameters. Process variation and mismatch are modeled as statistical parameters.

Employing SPICE simulations in background, a sensitivity analysis identifies the parameters impact on the circuit performance cost function. In Worst-Case Operation Analysis, different operating conditions are systematically varied to determine the worst-case operating conditions. Statistical analyses in WiCkeD consider these conditions for realistic yield estimation, where every sample should meet specification across the whole operating range to be considered successful design.

As an alternative to Monte Carlo sampling, the WiCkeD tool can employ the efficient worst-case distance method to measure robustness. Using the sensitivity methodology, the statistical parameters are varied in a deterministic way searching the most probable set of statistical parameters for which a performance specification fails. This enables the determination of the worst-case distance, a measure for yield and robustness in multiples of sigma.

WiCkeD includes optimization tools that iterate on a process of obtaining sensitivities, adjusting design parameters to achieve performance improvements. The tools handles trade-offs with multiple performances across the whole range of operation conditions. At statistical level, design centering or yield optimization maximizes robustness and yield respectively.

An entire verification flow is available by using scripting to combine WiCkeD analysis tools to systematically check performances at worst-case operating conditions and statistical variations efficiently and effectively. The flow is made of a sequence of analysis steps which are interrupted if a fail is detected:

1) Nominal Simulation
2) Worst-case operation analysis (WCO)
3) Monte Carlo analysis (MCA)
4) Worst-case analysis (worst-case distance) (WCA)

III. Application and Simulation Results

The proposed methodology was tested on horizontal porting of a typical Bandgap Voltage Reference [15], as shown in Fig. 3, between two 180μm/1.8V technology processes. The motivation for choosing this scenario was primarily twofold: firstly, a bandgap voltage reference is an essential building block in many designs; secondly, horizontal porting is important when moving between foundries or even at same foundry but different process variants at same node, where the major impact are in electrical properties of available devices. The porting flow can even be applied to make a more solid technology selection by comparing functionality and robustness of a design in different technologies.

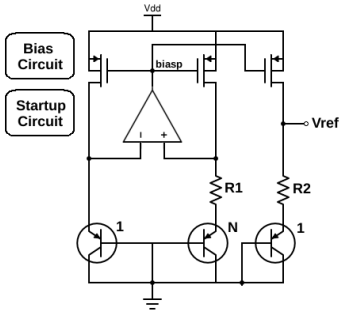

Fig. 3. Schematic of the Bandgap Voltage Reference used as study case.

A. Porting the schematic

For MOSFETs and resistors an equivalent match was found between source and target PDKs, and their sizes were kept unchanged. Yet for bipolars, which normally have a fixed emitter area, no exact correspondence was found in the target PDK. In the original schematic, the PNP used had an emitter area of 2μm X 2μm, while the minimum PNP available in the target PDK had a larger area of 3μm X 3μm. This difference will likely impact the new schematic performances.

At this point SPT was invoked with the conversion rules. The migration of 49 cells, considering hierarchy, lasted only 2 seconds. The schematic was updated with the target PDK cells, properly sized, and a report was generated with details of the porting process.

B. Design Assessment

The goal, in this step, is to adjust the circuit manually to ensure proper work of the new schematic. The simulation results of schematics on both source and target PDKs are summarized on 2^{nd} and 3^{rd} columns of Table I, respectively. We observe small variations of most specifications, except for the large increase of temperature coefficient, TC.

Further investigation indicated a non-linearity on the behavior of TC. In order to tune that, before proceeding to the verification step, the resistor values were adjusted by parametric analysis. New simulations results are summarized on 4^{th} column of Table I. Improved temperature coefficient and reference voltage at the output, V_{ref}, are seen, but an increase on the current consumption, I_{cons}, is observed as well. This result is not surprising, considering the increase in the emitter area, which has a direct impact on the current flowing through the bipolar transistor.

TABLE I
Comparison of simulation results

Design Specifications	Source PDK	Target PDK	Target PDK with design assessment
V_{ref} @ 27°C (V)	1.208	1.190	1.207
TC (ppm/°C)	8.41	55.76	17.82
PSRR @ 0Hz (dB)	-59.24	-54.31	-54.7
I_{cons} (μA)	4.97	4.88	10.19

C. Robustness Verification

Having ensured the new schematic works properly at nominal conditions, we need to ensure functionality at worst case operating conditions and consider process and mismatch variations, as explained in II-B, with the use of WiCkeD.

On a first run of the verification flow, results showed that the temperature coefficient was largely out of the specification, at the lower limit of VDD, as shown on Table II.

TABLE II
1^{st} Verification results

Performance	Spec.	Nominal	WCO	VDD (V)	Temp (°C)
V_{ref} (V)	>1.184	1.208	1.203	1.62	125
	<1.232		1.208	1.98	6.6
TC (ppm/°C)	<40	17.82	837.4	1.62	-
PSRR (dB)	<-40	-54.7	-44.94	1.62	125
I_{cons} (μA)	<15	10.19	13.66	1.8	125

With a sensitivity analysis and parameter sweep, it was possible to identify which MOS transistors had most impact on the worst-case operating condition of TC. After changing the dimensions of two NMOS that aggravated the TC, the final improved result was 18.32ppm/°C, at lower limit of VDD. New results for all the performances are shown on Table III.

The results of a new verification flow are summarized on Table III, including those of the Monte Carlo (MCA) and Worst Case Analysis (WCA).

TABLE III
2^{nd} VERIFICATION RESULTS

Performance	Spec.	Nom.	WCO	MCA/ Yield	WCA sigma/ Yield
V_{ref} (V)	>1.184	1.207	1.203	100%	3.82
	<1.232		1.207	100%	5.42
TC (ppm/°C)	<40	16.83	18.32	100%	4.76
PSRR (dB)	<-40	-53.95	-44.56	100%	>9.3
I_{cons} (μA)	<15	10.19	13.66	100%	3.99

For all the performances, MCA results showed a yield of 100%, for 200 samples, with the performances distributions shown on Fig. 4. For instance, the temperature coefficient had a mean value μ=18.33 ppm/°C with a robustness σ=4.15. WCA results showed that all specifications could be achieved with a robustness level of at least 3.82σ.

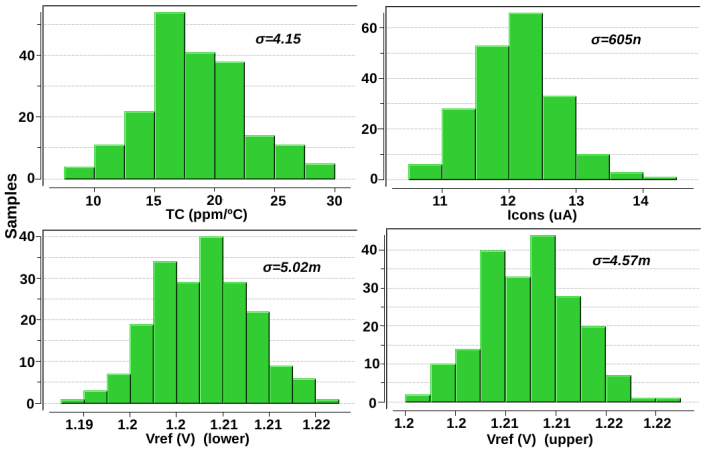

Fig. 4. Performance distributions of Monte Carlo Analysis.

IV. TIME EFFORT DISCUSSION

For this paper's porting example, a total amount of 6h was needed up to the final verification, using two CPUs simultaneously. The effort on the migration step consisted mostly in generation of the conversion rules file, which took approximately half an hour for the bandgap reference example. Depending on the size of the PDK or the number of cells needed, this step may take longer. Still, it is required only once for each source-target PDK pair and can then be applied to thousands of blocks without additional effort. The schematic porting itself took only 2s.

The design assessment step can vary much depending on the type of porting, horizontal or vertical. In the horizontal case, often no changes are needed if adequate cells are available in the target technology and it's sufficient to run the automated verification flow.

If the porting is vertical, or when respective cells are missing in the target technology, it is common that topological changes are needed, i.e. on bias or supply voltage, therefore this step may last longer. For this paper's example, design assessment took approximately 30 minutes.

The final step, which includes both verifications and the manual optimization, required approximately 3800 simulations and lasted up to 5 hours. If one desires numerical sizing, exploring features of WiCkeD optimization tools, for example, the effort for this step will greatly increase.

V. CONCLUSION

In this paper, a new procedure for technology migration was proposed, with the use of MunEDA tools. In this method, schematic porting is automated and much faster than manual porting. The methodology was tested on a bandgap reference voltage, and simulation results of the three steps were presented. The final design achieved a robustness level of 3.82σ, in less than one work-day.

ACKNOWLEDGMENT

This work was partially supported by CNPq, FINEP, CI-Brasil Program and MunEDA GmbH.

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