International Cooperation Forum

Automotive IC-Design
Challenges – Strategies – Trends

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Robustness and Reliability -
Facing new Quality Levels for Automotive ICs
with Design for Yield

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MunEDA Company Overview

- Company Start 2002
- Spin-off from EDA Institute of Munich Technical University
- Worldwide Team: > 25
- Worldwide Sales & Support: Europe, USA and Taiwan
- WiCkeD*: Silicon proven DFM-DFY-DFR EDA Software Solution

*In USA also DesignMD
Functionality covered by automotive electronic systems

- Convenience Electronics
- Driver Information
- Communication
- In-car entertainment electronics
- Automotive Safety

► 25% average car value comprises of electrical & electronical components in 2005 → half of this: semiconductors
Automotive Semiconductor Market – stable growth

$16 billion in 2004 will rise to $25 billion in 2009 at an average annual growth rate (AAGR) of 9%.

- MOS micro ICs: 63%
- MOS memory: 37%

Source: BCC Research
Semiconductors in Automotives

Discrete & Optoelectronics
- IGBT
- Power MOSFET
- Power Management
- Transistor
- IGBT Power, Bipolar, FET, MOSFET, Small Signal
- Bipolar, Power MOS
- Diode Rectifier
- Varistors
- Optoelectronics LED

Logic ICs

Micro ICs & ASIC

Memory ICs
- SRAM
- DRAM
- Flash
- EEPROM
- MRAM

Analogue & Mixed-Signal
- SDC
- Power IC
- ASSP

Sensors

► Need for accurate, closed-loop, real-time control, and processing of large volumes of data from multiple sensors
Robustness & Reliability

ICs/Circuits robust and stable against all influences, variations, failures, and defects in design, manufacturing, operation lifetime

► Goal: Maximum Yield & Sero-Defect-Rate
Business & Technology Challenges in Automotive IC Design

Business Challenges

- **Efficiency**
  - Low Price
  - Low Cost & Effort

- **Competitiveness**
  - Time to market
  - Time to Volume

- **Quality & Reliability**
  - Product Accuracy
  - Design & Production Reliability

- **Delivery**
  - High Volume
  - Yield & Robustness

Design Challenges

- **Design Efficiency**
  - Time to Production

- **Design Complexity**
  - Process aware design

Influenced by

- Design effort
- Design cost
- Respin quota
- Design time
- Design quality
- # Redesigns
- SoC
- Mixed-Signal
- Technology shrink
- Process variations
- Operating conditions
- Design specifications

► Design & Manufacturing effort, time, reliability and yield main success drivers for automotive ICs
Customer goals for automotive IC design

„8% efficiency improvement per year!“ *

⇒ i.e. design projects in 2010 require in average only 60% of today‘s design time & effort

Effects ?!

• More time for running design projects
• Lower design cost
• Less bottle-necks in design projects
• Higher number of simultaneous design projects possible with same resources

* Customer management
Customer reality and vision

Customer IC project duration reality today (2005): ∅ 19 Months

- Main influence on design time efficiency: Redesign

Customer Vision & Targets for IC Design & Manufacturing 2010:
- First time silicon right!
- Redesign only in very exceptional cases!
- Multiple Redesigns not permitted!

Target: - 33%
IBM quote: „3 months delay equals 500M$ loss!“

Source: Cadence, IBM
Technical influence parameters on automotive IC designs

Integration Level:
- System-on-chip (SoC)
- Mixed-Signal
- System-Level
- Block-Level
- Redundancy

Technology Level:
- Nano-Technologies
- Process Variations
- Mismatch
- Dependencies
- Correlations,

Constraints & Performances

Level:
- Sizing Rules
- Gain
- Power
- Phase, Phase Margin
- Frequency, Noise
- CMMR, PSRR, …

Operation Conditions

Level:
- Temperature
- Supply Voltage
- Load
- Voltage-/Current-Stability
- Aging, Failure Safety,…

► Existing and new design challenges require innovative and enhanced design, sizing and optimization methodologies
Design of block-level components – using DFM DFY DFR methodology

Time to market

Customer requirements

Microchip-Development
Design → Layout

Microchip-Production
Fab → Test

Sales
Trash

Design of block-level components

Topology design
Change of Device Parameter (Sizing)
Simulation

Until now by hand
Design of block-level circuits – using DFM DFY DFR methodology

(time to market)

Microchip-Development
Design
Layout

Microchip-Production
Fab
Test

More Sales
Higher Yield
Less Trash

Design of block-level components

Analysis and optimization (sizing) of circuits on block-level using MunEDA DFM DFY DFR technology

By factors faster and much more efficient

Customer-requirements

Topography-design
Need of new design methodologies for automotive ICs

Methodology

DFM
Design for Manufacturability

DFY
Design for Yield

DFR
Design for Reliability

Target

Functionality
Yield, Volume
Reliability

Focus on

IC Design
IC Manufacturing
IC Operation

Effects

- Effort (time&cost) reduction
- Design accuracy
- Time-to-production
- Yield improvement
- Cost reduction
- Delivery safety
- Reliability
- Failure safety
- Robustness

► All three issues DFM, DFY and DFR can have definitive & decisive influence on circuit design
### Application Field | WiCkeD Features
--- | ---
**DFM – Design for Manufacturability** | - Circuit Structure Recognition & Analysis  
- Constraint Management  
- Feasibility Optimization  
- Sensitivity Analysis  
- Nominal Diagnosis & Performance Optimization

**DFY – Design for Yield** | - Monte Carlo & Yield Analysis  
- Yield Optimization & Design Centering  
- Worst Case & Correlation Diagnosis  
- Mismatch Analysis

**DFR – Design for Reliability** | - Worst Case Operation  
- Operation Condition Influence Analysis & Optimization  
- Design reliability & accuracy analysis

*WiCkeD: Worst Case Distances*
MunEDA Applied to Customer projects and technologies

Circuits:
- Adiabatic Logic Gates
- Bandgaps
- Buffer chains
- Bypass Filters
- Cascode Gain Stages
- CCOs
- Charge Pumps
- CML Converters
- Comparators
- Constant Voltage Sources
- Current Mirrors
- Current Sources
- Current Mirror OpAmps
- Differential Amplifiers
- Filters
- Folded-Cascode OpAmps
- Fully Differential OpAmps
- High Voltage Circuits
- Latches
- Level Shifters
- Low Voltage Circuits
- Operational Amplifiers
- PLLs
- Receivers
- RF-Circuits
- Ring Oscillators
- Sens Amplifiers
- Sensor Circuits
- Single-Stage Amplifiers
- Transceivers
- VCOs

... and more

Technologies:
- 500n
- 350n
- 180n
- 130n
- 90n CMOS
- First projects in 65n CMOS started
- BiCMOS and Bipolar

Proven in more than 250 design and tape-out projects since 2002
IC: Operational Amplifier used as Voltage Regulator in automotive communication system

Task:
Original circuit manufactured in 180 nm process technology. Design reused, resizing & yield ramp up for 130 nm.

DFM / DFY - Solution:
In three steps from 0% to 99% Yield

Successful Yield ramp up for new technology in 30 min simulation time!
IC: BiCMOS operational amplifier for automotive applications migrated to a new technology with e.g. bipolar gain being lower than with older technology.

Status: Specifications are not fulfilled, especially not the open-loop gain, A0.

**Task – DFM-DFR Approach:**
Within two steps to a robust and reliable design:

1. Fulfilling constraints and sizing rules
2. Nominal circuit optimization

**Result:**
Specification are now fulfilled for nominal process and operating conditions. Further yield optimization results in high robustness against temperature & voltage supply variations.
Customer Example 3: Design Time & Effort Reduction

IC: Transimpedance Amplifier for automotive optoelectronic system designed for 350nm process technology.

Problem:
- Tough operating requirements specified with high bandwidth and stability.
- Performance maximization showed too complex task for manual design. Automated DFM, DFY & DFR methodologies applied.

<table>
<thead>
<tr>
<th></th>
<th>Start</th>
<th>Previously Sized Manually</th>
<th>WiCkeD (1.5MHz)</th>
<th>WiCkeD (4 MHz)</th>
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<tbody>
<tr>
<td>Design Time</td>
<td></td>
<td></td>
<td></td>
<td>1 day</td>
</tr>
<tr>
<td>Bandwidth† (MHz)</td>
<td>0.38</td>
<td>1.5</td>
<td>1.5</td>
<td>4.0</td>
</tr>
<tr>
<td>2nd Pole (MHz)</td>
<td>83</td>
<td>250</td>
<td>500</td>
<td>457</td>
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</tbody>
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† Bandwidth optimized while maintaining a minimum gain of 60dB

Benefits:
- Significant design time savings
  - Sizing time from 4 weeks to 1 day
- Performance & robustness improvement
  - Bandwidth increased from 0.38 to 4.0 MHz
  - Second pole raised from 83 to 457 MHz
Customer Project Example 4: Time to Volume Improvement

- Circuit: Voltage reference in a flash memory product
- Key issues: Low power, Vth mismatch, non-linear temperature curve
- Yield on first silicon 20% even after trimming, due to parametric failures

Application of MunEDA technology:

- **Conclusion:**
  
  With DFM-DFY-DFR: „First silicon right“.

- Yield Optimization: Fully automatic improvement from 20% to 83% parametric yield.
- Parametric yield improvement confirmed by second silicon.
- Indication for further topological change: expected yield after modifications: 93%.
MunEDA: DFM DFY DFR - Benefits for Circuit Design and Manufacturing

- DFM - Reduce IC design time & cost
- DFY - Maximize IC yield & volume
- DFR - Guarantee IC reliability & robustness

Main Goal: First silicon right
Reduce cost and speed up time-to-market!