Systematic Analysis & Optimization of Analog/Mixed-Signal Circuits Balancing Accuracy and Design Time

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ABSTRACT

In this paper we will demonstrate the benefits of systematic circuit analysis and optimization applied at different abstraction levels of a typical analog and mixed-signal design to address market requirements and technical challenges of nanometer technology nodes. The paper emphasizes the systematic approach using automated analysis and optimization technology in comparison with the still widely spread manual analog design approach led by designers intuition. We chose a double ring oscillator consisting of a Main PLL and a Dither PLL as example to demonstrate how such systematic methodology can even handle large circuits.

1. INTRODUCTION

For many years the shrinking process technologies have brought benefits such as increased circuit complexity and reduction in cost, size, and supply voltage. However, this has also caused difficulties for analog circuitry. This was managed by relaxing size limitations of the analog parts and implementing additional safety buffer, but there are two factors which make it more and more difficult to manage further shrinking of analog circuitry: the decrease of supply voltage and the increasing impact of process variations.

Despite all of the efforts to reduce process variations they can not be reduced at the same pace as the process dimensions, and as a consequence their relative size and the impact is increasing with every new technology node. The impact of statistical process variations and operating conditions on the circuit performance has become so significant, that statistical analysis is no longer considered a nice-to-have feature. In today's nanometer technologies this is becoming a must-have functionality, and foundries provide data about statistical process variances for most technology nodes below 130nm.

At the same time market requirements in terms of performance, complexity, and design time, are making the traditional design approach of manual intuitive sizing and verification by simulations less feasible. Systematic tools based design can handle larger design complexity with a large number of design specifications at once. Systematic targeted sizing tools increase productivity and achieve more thorough verification coverage including process variations to avoid silicon failures.

2. Problem Formulation and Circuit Description

To demonstrate the methodology we have chosen to optimize a double ring oscillator consisting of two PLL cells, a main PLL and a Dither PLL. The oscillator is used as an IP block within a mixed-signal circuit which is a complete 24-bit, single chip, D/A converter and power filter amplifier for car audio applications. A programmable PLL needs to lock at the input frequencies of 64*Fs and 50*Fs with Fs=48KHz for all the input configurations.

With the given architecture we are addressing a electromagnetic interference (EMI) problem of traditional clock generators: due to the high output edge switching rate which requires to reduce their impact.

Through the technique named dithering, the harmonic peaks amplitude can be reduced by a clock frequency/phase modulation. In this way, the spectrum of the dithered clock presents several peaks around the fundamental and the harmonics of the frequency clock respectively, as shown in Fig. 1

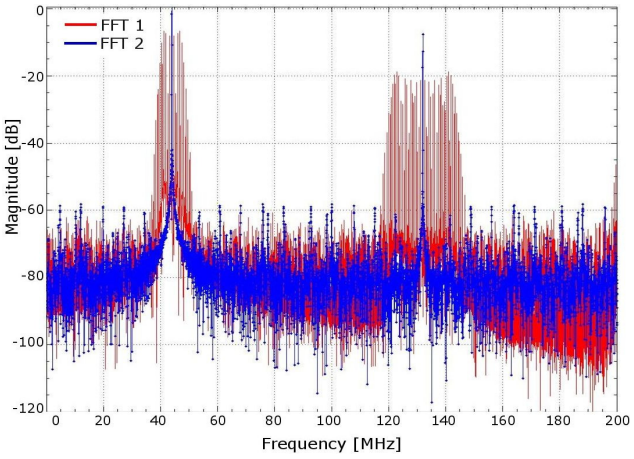

Fig. 1 Spectrums of the non dithered clock FFT 2 (blue/black) and the dithered FFT 1 (red/gray)

It can be seen that the peak amplitudes of the dithered clock (red/gray line) are less than the ones of the not dithered clock (blue/black line), improving the EMI performance.

The clock generator architecture [1] (see Fig. 2) is composed of two PLLs: the main PLL working at the fixed clock frequency and a dithered PLL at the modulated clock frequency. Both PLLs have the same ring oscillator.

The dithered ring oscillator is biased by a replica of the main ring oscillator current added up to a mismatch compensation current and a triangular wave current, which modulate the oscillation frequency. Consequentially, the dithered clock determines the DSP frequency and the DSP output (audio data) is dithered.

Then, a data synchronization phase, at the not dithered clock is done.

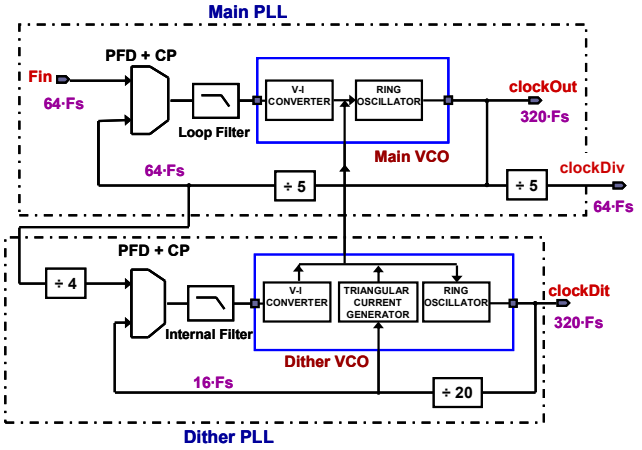

Fig. 2 Schematic block of the double ring oscillator dithered/non-dithered clock generator

The specifications which should be analysed and optimized have to be formulated and written separately for the main and dither VCO's.

For the main VCO, the voltage tuning range operation (VF) is included into the range between 2V and 3V while the closed loop oscillation frequency is F_{VCO} = 320*FS =15.360MHz. To guarantee the lock of the VCO for VF=2.0V the output frequency must be lower than 15.36MHz and for VF=3V the output frequency must be higher than 15.36 MHz.

For the dither VCO, it is needed to guarantee that the average oscillation frequency is equal to F_{AVG} = 320*FS = 15.360MHz and the phase difference between main clock and dithered clock is less than $\pi/2$.

The above formulated phase difference is mandatory to keep synchronization between main and dithered clock. This last constraint should be formulated by the equivalent expressions in the period of the dithered signal, also visualized in Fig. 3:

$$TMAX - TAVG < 7.23 \text{ ns} \quad (1)$$
$$TAVG - TMIN < 5.92 \text{ ns} \quad (2)$$

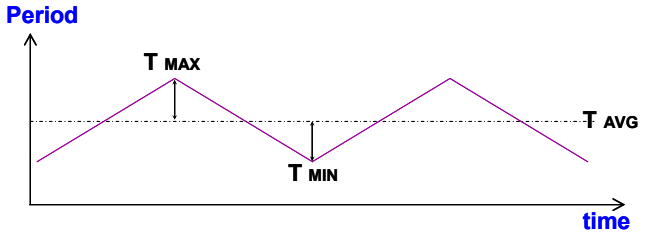

Fig. 3 Dithered clock period

This problem is well suited to demonstrate both, the systematic and targeted sizing algorithms in WiCkeD™ as well as the usage of different abstraction levels.

3. Hierarchical approach

Since both, systematic sizing approaches and statistical analysis, require many simulations, we apply a hierarchical approach with different levels of simulation and accuracy from system to transistor level to balance the tradeoff between time and accuracy.

The general approach can be described as follows:

1) The circuit is partitioned into multiple blocks.
2) For each block a Response Surface Model (RSM) [2] to characterize the performance over design, process and operating parameters is created to speed-up all the following circuit analyses & optimizations.
3) Uncritical blocks are replaced with the correspondent behavioural code which can be characterized (and extracted) over deterministic, operating and process parameters by WiCkeD RSM modelling based algorithm for analysis & sizing, while critical blocks are kept at transistor level.
4) Circuit is simulated at transistor level using fast spice simulators to get adequate compromise between speed and accuracy.

4. Technology used

We used ELDO® [3] from Mentor Graphics for transistor level spice simulation and the ADVance MS™ (ADMS) mixed-signal simulator [4] from Mentor Graphics® for behavioural code simulations.

All sizing and optimization steps were driven by WiCkeD [5], an EDA environment independent tool for circuit analysis and sizing. While WiCkeD is mostly known for statistical optimization with a unique deterministic worst-case distance algorithm, the same optimization functionality can be applied efficiently and effectively in all sizing tasks such as nominal design, and as shown in this work also at different levels of abstraction.

The WiCkeD workflow starts with a systematic analysis of circuit behaviour and based on this the design parameters are adjusted for targeted optimization. All design parameters and all specifications are considered at the same time, while monitoring design constraints and ensuring the functionality over the entire range of operating conditions. This can be applied to nominal design as well as statistical optimization to improve yield and circuit robustness, when statistical data is available.

For circuit simulation WiCkeD executes the same simulators in batch mode that designers use and it analyses the simulation results. Therefore it can be applied for any kind of simulation with a batch mode capable simulator, regardless of simulation level or even application domain. The computational effort for analysis and optimization depends on the effort for each simulation. After WiCkeD executes an initial set of simulations to performs a baseline analysis of circuit behaviour, this information can be visualized for a circuit designer as well as processed by WiCkeD's optimization algorithm. The targeted optimization is applied to all circuit perfomances with the goal of reaching all specifications or maximizing certain performance values as specified. During such optimization of all specifications simultaneously WiCkeD typically regains the effort spent on the initial analysis and saves overall effort, especially for complex circuits, while providing parameter values optimized with regard to the specifications.

WiCkeD's statistical optimization follows the same workflow, except that the design goals are not the specifications itself, but the so called worst-case distance of the design point to each specification. The worst-case distance is a measure for yield and reliability. Each worst-case distance is measured in multiples of the process variation sigma, making it independent from performance dimensions and well suited for maximizing the overall circuit yield and reliability. The deterministic worst-case distance analysis algorithms used to measure the worst-case distance require significantly less simulation effort for calculating yield than monte-carlo based methods, and beyond calculating it, WiCkeD provides the required information how the yield and robustness can be improved, which monte-carlo analysis does not provide. Based on this, WiCkeD enables and guides systematic optimization, providing design centering capabilities with manageable effort [6,7,8,9].

5. Circuit Analysis & Yield Optimization

The goal of this project was to optimize the circuit under consideration of the process and operating variations, while not consuming more time than traditional manual design would require for nominal sizing only.

The combination of the systematic and targeted sizing algorithms in WiCkeD and the different levels of abstraction enables unprecedented flexibility to balance between simulation accuracy while saving design time. The following design flow has been applied to achieve the desired results:

1) Systematic analysis & optimization of the free running Main VCO (V-I Converter, mirrors, ring oscillator) at transistor level in open loop to achieve high performances and robustness despite the impact of process and operating parameter variations. This analysis & optimization took around two minutes using WiCkeD, so that a deep circuit analysis and optimization could be done with high accuracy in short time.
2) Systematic analysis & optimization of closed loop Dither VCO (Triangular wave current generator) over the process and operating parameters and its impact on the entire double ring oscillator dithered/not dithered clock generator. When tuning the dithered PLL the specification can only be simulated by simulation of the entire double ring oscillator. Using transistor level simulations, each run would consume 4 hours, which would make the systematic analysis cumbersome and statistical optimization even unfeasible. To speed up simulation times from 4 hours to 4-5 minutes a mixture between behavioural or numerical models and transistor level simulation is applied to get the best compromise between the desired accuracy and simulation effort to impact the design time quality and efficiency to cope with possible circuit limitations and weak points before going to silicon.
3) Verification of the results achieved in step 2 through simulation of the corner models at transistor level. This verification requires 3 times 4 hours.

Please note, that for the verification in step three the long simulation time is needed only once to validate the result from step 2 after it was found. Actually finding this result would not be feasible only with a circuit simulator. This requires sizing tools such as WiCkeD.

5.1 Main VCO Analysis & Optimization

The free running Main VCO analysis & optimization is demanded to guarantee that the following performances (3,4) and dc constraints (saturation, inversion) are fulfilled at the same time over the process and operating parameters variations:

$$FVCO(2.0)<15.36MHz \quad (3)$$
$$FVCO(3.0)>15.36MHz \quad (4)$$

The temperature variation on which the circuit is required to work properly ranges from –40°C to 150°C. The capacitance variation plays a key rule in the optimization. We emulated the capacitance variation during yield optimization by applying a small trick: In a first optimization run we defined it as a design parameter to optimize the nominal value, and then defined it as operating parameter to emulate the capacitance variation during yield optimization.

The above mentioned flow is shown in Fig. 4. As it can be seen, before running the optimizations (feasibility optimization for dc operating point and nominal optimization for performances), sensitivity analysis and worst case operating analyses have been done to deeply check circuit performance sensitivities with respect to design and operating parameters.

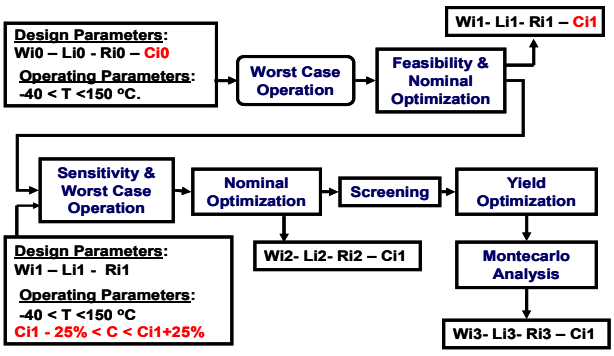

Fig. 4 WiCkeD design flow for the Main VCO

This is a key point before running any optimization, because it allows designers to become much more confident with any possible circuit weakness.

The dc operating point optimization is needed because the VCO used topology includes a voltage to current converter topology, which consists of an operation amplifier and some current mirrors that must operate in saturation region, while the ring oscillator topology requires for some specific analog transistors to operate in saturation as well.

In Fig.4, the followed methodology showed that after Feasibility & Nominal Optimization, the first design parameter set (Wi1, Li1,..) has been found which fulfill the dc operating point and specifications in typical and worst case operating conditions. Then, to overcome the lack of statistical models for the capacitor, the optimized capacitance value has been used as an operating parameter for next analyses and optimizations in order to get a reliable and efficient methodology which should cover the possible process variations. As can be seen, after the nominal and yield optimization a new design parameter set is provided by WiCkeD, because the nominal optimization provides the best performance values without taking into account process parameters, while the yield optimization (when it is needed), moves the design parameters set to try to maximize the worst case distances to increase the design yield and robustness.

Furthermore, it is important to point out that while going to deep sub-micron technologies, the short channel length and the low threshold voltage values are making the higher order effect strongly impact the performance behaviour with respect to the operating parameters, whose behaviour is often showing a quadratic effect behaviour. Consequentially, the usual corners analysis becomes too optimistic for the operating conditions, as the worst case operating points may not be in the corners due to nonlinear behaviour. For this reason WiCkeD's operating analysis algorithm is based on a second order approximation together with sensitivity analyses for detecting the real worst case operating point. This analysis provides the real worst case operating point for each performance to better evaluate and achieve the best performance values over the typical and worst case operating conditions.

The final yield results were verified by Monte Carlo analysis available in WiCkeD environment, as shown in Fig. 5,6.

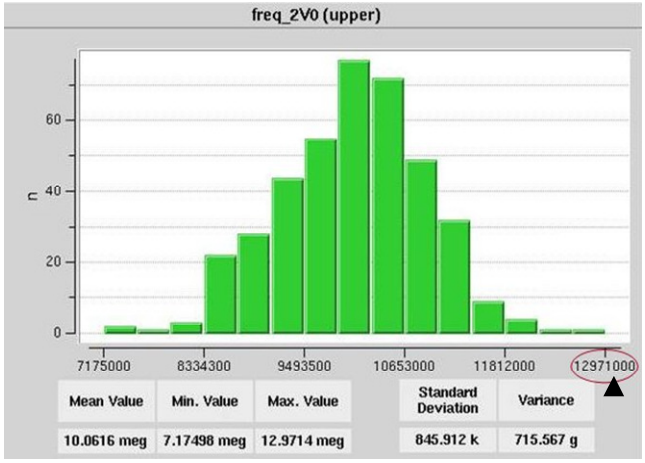

Fig. 5 Monte Carlo analysis results for F_{VCO}(2.0) in worst case operating conditions

The optimized Main VCO results have been cross-checked with transistor level simulation (Eldo) through corner analysis. Fig. 7. shows the VCO characteristic at typical conditions and the different corners in worst case operating conditions, fully confirming the WiCkeD results in figures 5 and 6.

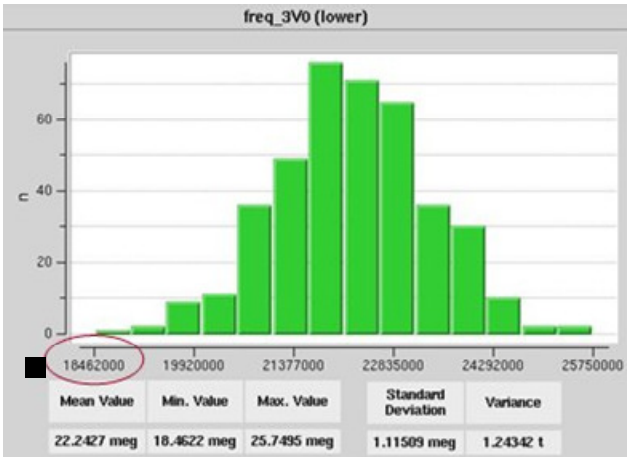

Fig. 6 Monte Carlo analysis results for F_{VCO}(3.0) in worst case operating conditions

It is important to point out that the usage of the so called fast spice simulator, which enable the full chip simulation with all blocks at transistor level, was not needed because the Eldo simulation results fulfilled all the specs in advance. Note that the corner analysis is used as reference because it is more commonly known. When time accurate statistical models are available, non oversized circuits can be achieved with better circuit characterization before silicon including correlation among process parameters.

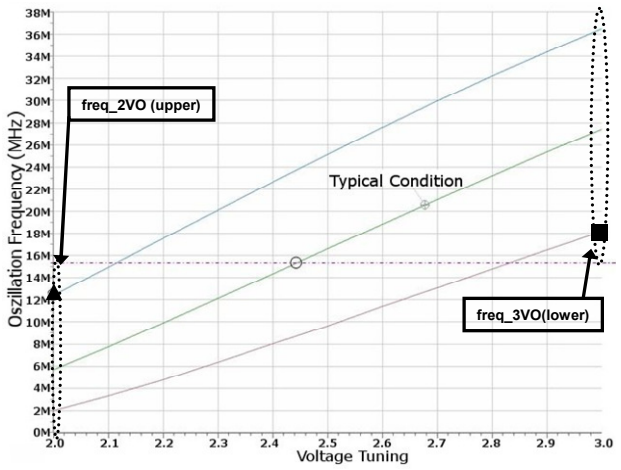

Fig. 7 Free running Main VCO: typical (green, middle) and worst case (red and blue, upper and lower) simulation results

The Dither VCO analysis and optimization can not be performed with the whole circuit at transistor level (PLLs, references) because each simulation takes around four hours using spice-like simulators, which is not feasible, neither for design purposes nor with a view to perform an optimization.

A methodology which should guarantee the best compromise between speed and accuracy needs to be put in place to characterize the whole circuit. The possibility to manage environment blocks at different level of abstraction inside WiCkeD allows to combine different levels of simulation to get a reliable and robust circuit in a short time. This has been done in two steps:

First step: to drastically reduce the simulation time, behavioural description for non-critical blocks (PFDs and dividers) was used, while the rest of the blocks were left at transistor level. Of course, this is only possible when the non-critical blocks don't have an appreciable impact on performance accuracy to maintain a good alignment with the same results at transistor level. The adopted solution reduced the simulation time in the order of 15min/20min,which is good, but still not enough to deeply analyse the circuit over the design, operating a process parameters variation.

Final step: to reach the optimum compromise between speed and accuracy, the Main PLL has been replaced with pulse and current generators, while the reference block (Bandgap) with a voltage source as shown in Fig. 8.

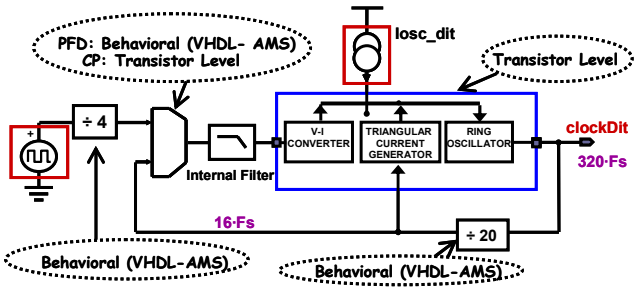

Fig. 8 Dithered VCO test bench at different level of abstraction

Through this, the simulation time was decreased to the range of 4-5min, which makes the required circuit analyses and optimization feasible in an appreciable timeframe while satisfying the requirements for a deep understanding of the circuit behaviour.

Circuit analysis and optimization was done with ADVance MS, featuring a single kernel simulator able to simulate the Dither VCO partitioned into a behavioural block, simulated by ADVance MS and analog blocks simulated by Eldo.

In this case, a different way to proceed would be the periodic analysis, which drastically reduces the simulation time too, but in this specific case two main bottlenecks came up with respect to the above mentioned solution based on ADVance MS: Firstly the simulation time reduced only to the range of 15 min, and secondly the designers faced convergence problems, so that a reliable and analysis was not possible.

The circuit performances should fulfill the target over the following operating conditions:

$C_0 - 25\% < C < C_0 + 25\%$
$I_{MIN} < IOSC\_DITH < I_{MAX}$

where IMIN and IMAX are the lower and upper current value generated by closed loop Main VCO in worst case operating conditions, while the lower and upper bounds for the capacitance value have been used based on the process design rules.

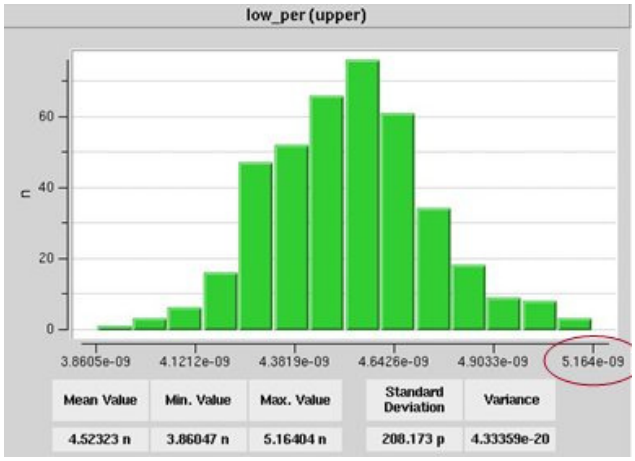

Fig. 9 Monte Carlo results for T_{AVG} -T_{MIN} in worst case operating conditions

As can be seen in Fig. 9 and Fig. 10, the Dither VCO specifications (1) and (2) have been fulfilled over the operating and process parameters.

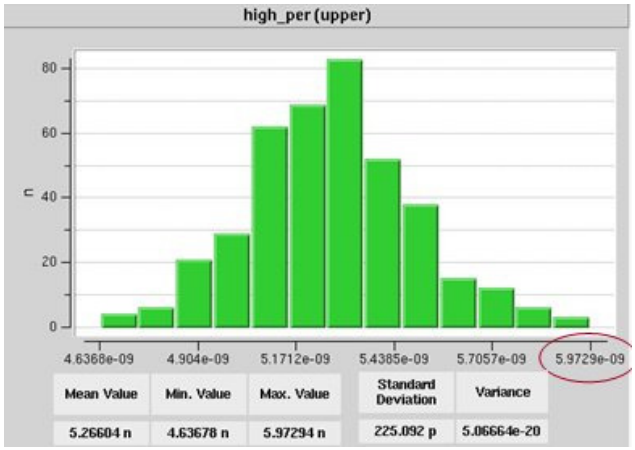

Fig. 10 Monte Carlo results for T_{MAX} –T_{AVG} in worst case operating conditions

The quality of the results has been verified using the optimized design parameters back-annotated onto the schematic and simulating the Dither PLL at transistor level. Table 1 displays the specifications (1) and (2) in the different corners at worst case operating conditions.

	T_{MAX} –T_{AVG}	Specification	T_{AVG} -T_{MIN}	Specification
Lower value	**3.140 ns**	**<7.23ns**	**2.737 ns**	**<5.92ns**
Typical	4.408 ns	**<7.23ns**	3.848 ns	**<5.92ns**
Upper value	**6.613 ns**	**<7.23ns**	**5.537 ns**	**<5.92ns**

Table 1 Eldo corners simulation results at worst case operating conditions

6. Benefits of this Methodology Based on WiCkeD Usage

The structured approach to circuit sizing by circuit analysis and optimization with WiCkeD provides two essential benefits: increased productivity and higher quality.

Even though the effort for setup and baseline analysis simulations is often used as argument against such structured approaches, WiCkeD has proved to be very efficient and significantly saved effort in the overall sizing process. WiCkeD can consider all specifications at the same time and especially when tradeoffs between multiple difficult specifications have to be made it converges efficiently toward the design goal, while designers can only focus on a limited set of specifications at once. For our PLL design we ensured all PLL design typical specifications such as phase noise in parallel to the ones covered in the previous sections.

Furthermore the structured approach is very thorough in terms of circuit analysis, providing a more holistic coverage than traditional analog design. While analog designers are generally concerned of losing control when using automation technology, our designers found the step by step interaction between WiCkeD and the user to be a natural extension of their design practice. Throughout all analysis and sizing steps WiCkeD consequently follows a glass-box approach, where the designer can monitor progress, fully control the optimization, make conscious tradeoffs based on thorough analysis data, and change design parameters after each iteration. While other sizing tools we have used confirmed concerns about the setup effort, convergence failure and distrust in results from black-box approaches, WiCkeD provided the functionality while the designers maintained control. This greatly improved the confidence in the circuit and the large amount of information we gathered from the different analyses (sensitivity, mismatch, worst case analyses) about the statistical influence (global and local effects) and the operating range enabled a better assessment of the circuit capabilities and impact of potential risk factors in advance.

For us, the availability of a tool like WiCkeD is a paradigm shift from traditional design, which is a combination of solving cumbersome complex equations and trial and error simulations based entirely on the circuit designers experience, to a structured analytical approach to circuit sizing.

Essentially a systematic and analytical approach to sizing analog circuits as provided by WiCkeD improves productivity, and with increased complexity and under consideration of statistical variations, it is becoming a necessity.

WiCkeD Monte Carlo Analysis provides plenty of statistical information addressed to check the main reasons of failure or circuit strange behavior. This can be done through a cross checking between data picked up from the parameter influence analysis which displays for each performance, the absolute influence of all the statistical parameters variance on the performance variance and the scatter plot feature, that enable for each sample the possibility to assess this node with the evaluated process parameter sigma distances from correspondent the mean values.

Moreover the consistency among parameter influence, scatter plot and Worst Case analysis results, provides a strong and really powerful methodology to deeply check the main reasons of circuit weakness and circuit failure before going to silicon.

7 Conclusion

The approach shown in this paper demonstrates a generalized method for systematic circuit analysis and optimization even for larger circuits. With a hierarchical approach and WiCkeD sizing tools we achieved the quality of statistical analysis and optimization, while saving about half of the time that traditional manual design would consume for nominal design only. Furthermore, the high quality nominal design results (yield 100%) also saved tim,e because the yield optimisation showed 100% yield after the first iteration, fulfilling all specifications.

The achieved results were validated by transistor level simulation results of the double ring oscillator and the design is now in production. The big advantage of using WiCkeD, apart of the saved time, it has been focused on the well proven quality and efficient design methodology put in place to reach at the first time the desired results.

The applied structured approach to circuit sizing introduces a paradigm shift from trial and error design based on simulation to targeted circuit sizing. Systematic analysis and statistical optimization methodologies address market challenges as well as the technical challenges introduced by technology nodes below 90nm, where statistical variations play an increasingly significant role.

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