

## Industry Application Examples

### Circuit Migration & Porting

- 16nm → 7nm – High-Speed Clock Generator Porting
- 28nm → 14nm – Schematic Porting of DDRx Interfaces
- 40nm → 28nm – Migration of IP for extreme low power dissipation
- 55nm → 40nm – Porting and Retargeting of Bandgap Voltage References
- 180nm → 150nm - Foundry-Technology-Platform Porting of ADC Buffers

### Circuit Sizing, Tuning & Retargeting

- 10nm – Yield optimization of High-Speed Transceivers
- 14nm – Batch Mode Sizing of FinFET FinFET General Purpose I/O & Memory Interface Macros
- 16nm - S&H Sample & Hold (ADC) Mismatch Analysis and Sizing
- 28nm - Performance & Corner Optimization of DDRx High-Speed I/O in FDSOI Technology
- 28nm - Path Delay Optimization of Receiver with 1300 Transistors for DRAM Memory
- 28nm - I/O Design Optimization Flow for Reliability
- 28nm – Standard Cell Design optimization and retargeting
- 40nm - Reliability & Yield Optimization of Relaxation Oscillator in Advanced CMOS Process Technology
- 40nm – read path optimization for speed and stability
- 130nm - Optimization of a Low-power Fully Differential OTA

### Circuit Analysis & Verification

- 10nm – FPGA CRAM cell analysis for 6.5 sigma
- 14nm – Fail analysis of Digital Temperature Sensors in Non-Volatile Memory
- 40nm – Debugging & Verification of 10bit SAR ADC
- 40nm – Process related yield debug and optimization of analog IP
- 55nm – PLL statistical analysis and optimization
- 65nm – 6T SRAM Bitcell Analysis for 6 sigma
- 65nm – Monte-Carlo analysis of 195k device High-Speed Clock Generator
- 90nm – Worst Case Analysis of matrix of sense amplifiers with 210k devices

## Selected Customer References



STMicroelectronics: “MunEDA WiCkeD is a substantial part of our reliability-based design flow for our CMOS and FDSOI technologies and extremely useful for design optimization of standard I/Os to meet tight specifications, ensure good design margins and reduce the design time dramatically” (MUGM 2015)



Infineon: “MunEDA WiCkeD WiCkeD has been seamlessly integrated in the design flow of Infineon for more than a decade” (MUGM 2013)



Samsung: “With MunEDA's tools for design optimization and statistical analysis of FinFET memory interface IP blocks we achieved an average reduction of design turnaround time of 50%, more than 6% performance improvement and up to 15% area reduction.” (MUGM 2013)



SMIC: “With MunEDA WiCkeD's optimization tools we have reduced the power consumption of an ultra low power reference voltage design for IoT applications by phantastic 40% down” (SemiWiki 2017)

Find more customer references at [www.muneda.com](http://www.muneda.com)

Contact MunEDA and our Worldwide Distributors at  
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## EDA Tools for Migration, Sizing and Verification of Custom IC Designs

MunEDA WiCkeD™ is the leading EDA software tool suite for IP migration & reuse, circuit analysis, and optimization of Custom IC designs (analog, mixed-signal, RF and digital).

MunEDA's solutions help customers to reduce design time and efforts.

Circuit design engineers analyze and optimize their designs with MunEDA tools to meet the specifications, to improve performance, robustness and yield, to reduce power consumption, area, and sensitivity to aging and degradation effects.

Circuit Schematic  
Migration & IP Porting

Circuit Sizing for Low  
Power, IoT  
Yield & Reliability

Circuit Verification for  
Variation, PVT, Monte  
Carlo, Yield & High-Sigma

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## Circuit Migration with SPT 2.0

MunEDA Schematic Porting Tool for circuit schematic migration and IP porting between different process technologies

## WiCkeD™ - Circuit Sizing & Tuning

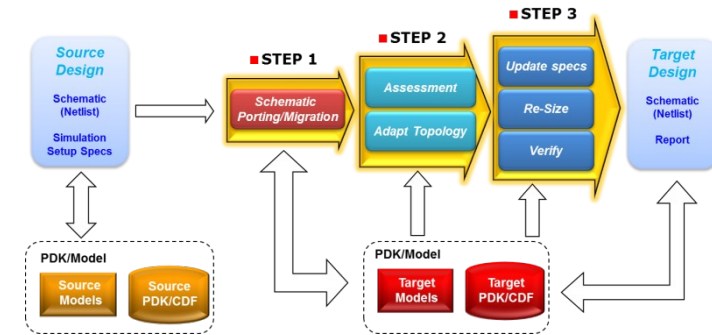
Meet performance specifications over all types of variation, design and operation parameters with MunEDA sizing & optimization tools

## Circuit Verification with WiCkeD™

Analyze and verify your circuit designs for constraints, performance specifications, operating and process parameters, global variation, mismatch and reliability

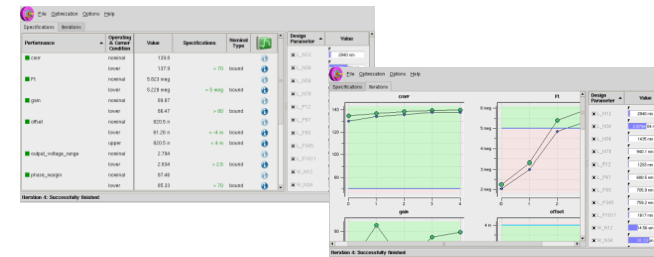
### Circuit Migration & Porting with MunEDA SPT

MunEDA SPT Schematic Porting Tool is part of a comprehensive solution for fast and reliable circuit migration & IP porting of custom IC circuits between different process technologies.



### Circuit Sizing & Tuning with MunEDA WiCkeD™

WiCkeD is a powerful optimization engine for automatic circuit sizing and optimization. WiCkeD improves circuit performance values, robustness, power consumption and area by changing design parameters with its highly efficient optimization algorithms. Main application fields include advanced analog/RF design, low power / low voltage design, as well as custom digital circuits.



### Circuit Analysis & Verification with MunEDA WiCkeD™

WiCkeD provides the designer with the most powerful Monte Carlo Analysis techniques for parametric yield analysis and interactive yield issue debugging with the smallest number of simulation runs.

With WCA the circuit designer is able to calculate statistical worst-case conditions of the circuit.



### Key features of MunEDA SPT Schematic Porting Tool

- Automated schematic porting within seconds instead of tedious manual work for days
- Easy setup by a convenient GUI interface for all operations by the user instead of error prone inhouse scripting
- Flexible property mapping with configurable rules
- Handles terminal name changes, different, extra or deleted terminals
- Handles different positions, placement and orientation of schematic symbols
- Customer & silicon proven with many different foundry PDK

### Key Features of WiCkeD™ Circuit Sizing & Tuning

- Supports FinFET and bulk technologies
- Explore trade-offs between power, speed, yield, and performance faster and better than ever before
- Tune circuits for better robustness by design centering
- Reduce design effort and design time
- Simultaneously handles multiple specs, tests, corners, and operating point constraints

### Key Features of WiCkeD™ Circuit Verification tools

- Constraint Generation / Editor / Management
- Sensitivity Analysis for geometries, environment, aging, process and on-chip variation
- Fast PVT & Operating Corner Analysis calculates influence of corner cases on given circuit performance metrics
- Efficiently combines corners to a minimum set of corner conditions to be checked
- Fast & Enhanced Monte Carlo Analysis (3-5 sigma plus)
- High Sigma Worst Case Analysis (6-9 sigma plus)
- Simultaneously handles multiple specs, tests, and operating point constraints
- Dynamic sampling
- Hierarchical sensitivities
- Interactive scatter plots and yield improvement