Improve Design Performance & Yield

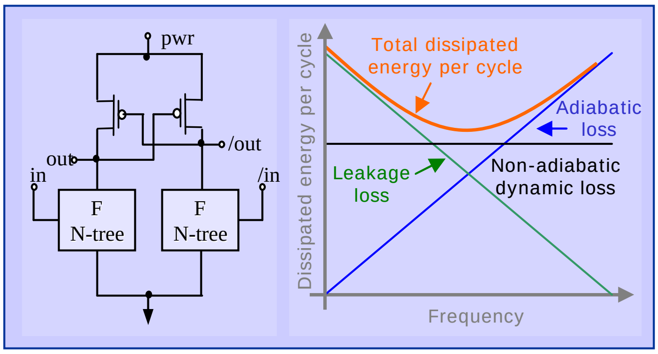
Power and Yield Optimization of Adiabatic Logic-Gates

Circuit & Application

Adiabatic logic gates for very low power applications. Process technology used was 180nm

Problem Formulation and Goals

Energy dissipation was increasing dynamic power and leakage current because of the growing number of transistors on a chip. However, the capacity of batteries did not increase in the same way. Energy dissipation of the adiabatic circuits relied on analog properties of the transistors. The design goal was to reduce power and increase robustness and yield.



Design Problems without WiCkeD:

- High power consumption
- Low robustness
- Low yield (40%)

Solution using WiCkeD

Step 1 – Nominal Diagnosis

The impact of device W/L ratio on energy dissipation showed different trends for each source of dissipation. Using WiCkeD's DFM Diagnosis the performance dependency and parameter redundancies were identified and clearly visualized. The designers were able to analyze the link between component values and power dissipation to modify the circuit interactively with WiCkeD.

Step 2 – Nominal Optimization

Circuit devices were sized by WiCkeD such that the power dissipation was as low as possible without lowering the frequency. The input signals were shifted by –90°.

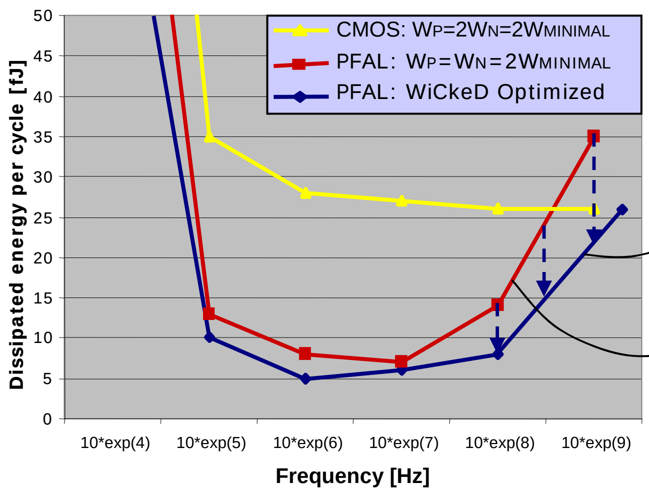
Step 3 – Tolerance Analysis and Worst-Case Diagnosis

The Tolerance Analysis measured the influences of the process variation of the circuit. Using this information together with the Worst-Case Diagnosis, designers were able to size the devices to maximize robustness with respect to the process variations.

Step 4 – Monte Carlo Analysis

Monte Carlo analysis validated the expected parametric yield the designers achieved with interactive design centering.

WiCkeD Results



Value added of using WiCkeD:

- **Power dissipation reduced 50%**
- **Crossover frequency over 1GHz**
- **Increased yield to ~97%**

WiCkeD Analysis and Optimization

Design before using WiCkeD:

- High power consumption
- Low robustness
- Low yield (40%)

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Corporate Headquarter
MunEDA GmbH
Stefan-George-Ring 29
81929 München, Germany
fon +49-089-930-86-330
fax +49-089-930-86-407
email info@muneda.com
web www.muneda.com

US Office
MunEDA Inc.
1250 Oakmead Pkwy, Ste 210,
Sunnyvale, CA 94085-4037, USA
fon +1-408-501-8858
fax +1-408-501-8859
email info@muneda.com
web www.muneda.com

Distributor Taiwan
Grand Technology Inc.
11F-1 No. 440 Chung Hsiao Rd
Hsin-Chu, Taiwan R.O.C.
fon +886-3-5622675
fax +886-3-5622676
email grandti@ms9.hinet.net
web www.grandti.com.tw

Distributor Korea
DAOU Xilicon Technology Co., Ltd.
4F Daehyun B/D, 273-1, Seohyun-Dong
463-824, Kyunggi-Do, Korea
fon +82-31-789-2800
fax +82-31-705-1199
email support@daouxilicon.com
web www.daouxilicon.com