

Circuit & Application

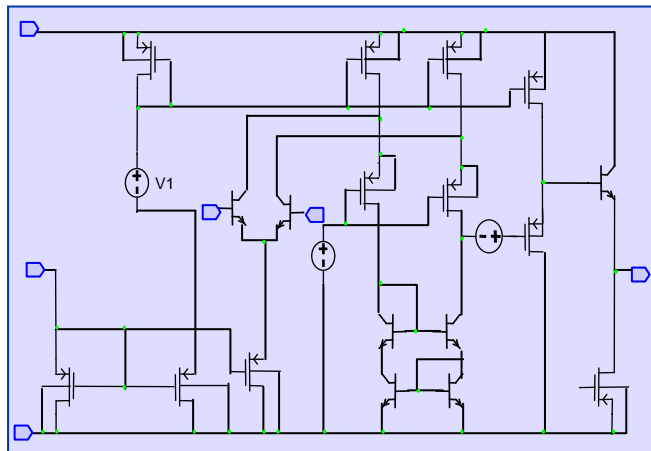
Folded Cascode trans-impedance amplifier used as IP in various other circuits with an open-loop testbench. Process technology used was 350nm.

Problem Formulation and Goals

The operating requirements for the circuit were to have a high bandwidth while maintaining a minimum of 60dB gain. Furthermore, the value for the second pole had to be high to increase stability.

Design Problems without WiCkeD:

- Increase bandwidth substantially
- Keep the gain at or above 60dB
- Shift second pole further right



Solution using WiCkeD

This design challenge included the frequent analog design problem of maximizing key performances while trying to minimize adverse impacts to other performances. The design flow using WiCkeD included three steps: circuit preparation utilizing automatic constraint analysis, achieving a feasible topology and optimizing performances.

Step 1 — Analysis: Circuit Preparation and Setup

WiCkeD's automatic constraint generation made it possible to quickly identify the current mirrors and level shifters. Additionally, the constraint analysis revealed that an auxiliary voltage source was needed. Furthermore, all design parameters (widths and lengths) for the devices the designer desired to be sized were identified as well as all performance parameters were defined at this step.

Step 2 — Feasibility Optimization

WiCkeD's Feasibility Optimization ensured all sizing rules were fulfilled. Additionally, the auxiliary voltage source was set in order to fulfill all constraints.

Step 3 — Nominal Optimization

By using WiCkeD's DFM Optimization, all circuit performances surpassed their specifications over the entire operating range. This improved the circuit characteristics and resulted in higher yield. Optimization time was minimized by using WiCkeD's parallel simulation capability distributing simulations onto various CPUs across the network.

WiCkeD Results

	Start	Previously Sized Manually	WiCkeD (1.5MHz)	WiCkeD (4 MHz)
Design Time		4 weeks	1 day	1 day
Bandwidth† (MHz)	0.38	1.5	1.5	4.0
2 nd Pole (MHz)	83	250	500	457

† Bandwidth optimized while maintaining a minimum gain of 60dB

Benefits of using WiCkeD:

- Significant design time savings
 - ⊙ Design time reduced from 4 weeks to 1 day
- Noteworthy performance gains
 - ⊙ Bandwidth increased from 0.38 to 4.0 MHz
- Dramatic robustness improvement
 - ⊙ Second pole raised from 83 to 457 MHz