MunEDA

Improve Design Performance & Yield

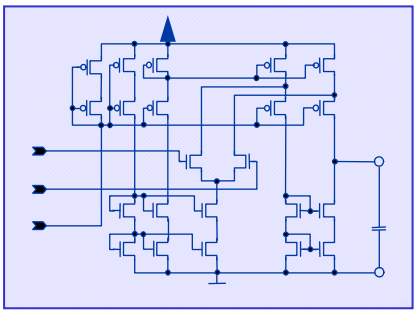
Folded Cascode Operational Amplifier: Design Reuse & Process Migration

Circuit & Application

Folded Cascode Operational Amplifier with 22 transistors for which designer selected to allow 44 design parameters to be sized. There were 9 process variation parameters and 4 operating condition parameters. Process technologies used were 180nm, 130nm, 90nm and 65nm.

Problem Formulation and Goals

The original circuit had been produced in 0.18µm technology. The devices needed to be resized to be reused for each of the smaller geometry processes (130nm, 90nm and 65nm). The designer's goal was to quickly find a feasible solution with optimal yield.



Main tasks of process migration:

- Meeting sizing rule constraints
- Resizing for design reuse to meet specs
- Yield Optimization for all process variations

Solution using WiCkeD

Based on specifications for each new process technology, the topology was analyzed with the initial sizing as start values. As expected, this resulted in 0% total yield and the circuit was not robust enough for the new process technology. WiCkeD used three steps to size the circuit for each new technology and achieved maximum yield each time.

Step 1 – Feasibility Optimization

Using WiCkeD's topology analysis and automated structure recognition, 190 sizing rules were automatically detected. WiCkeD's Feasibility Optimization aided the designer to match these rules and reach a feasible solution as starting point for the following performance and yield optimization steps.

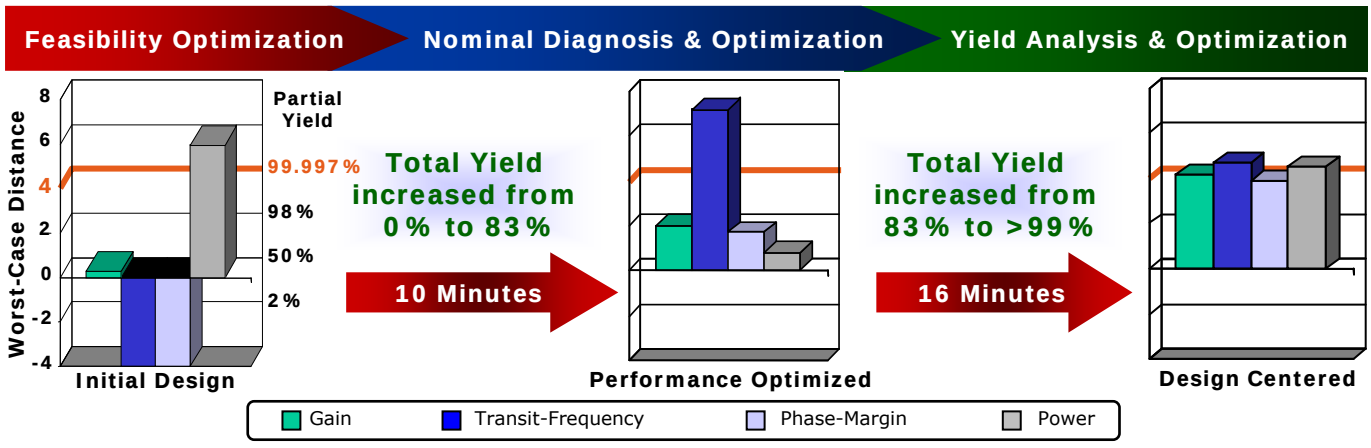
Step 2 – Nominal Optimization

WiCkeD's DFM Optimization brought all circuit performances to specification in 10 minutes of simulation using a deterministic optimization algorithm. Yield analysis of this performance optimized design showed an 83% increase in yield from the initial design.

Step 3 – Yield Optimization (Design Centering)

Using WiCkeD's Worst-Case Analysis, the designer was able to detect significant differences in robustness of the circuit performances. The partial yields of gain, power and phase margin were low. Using WiCkeD's Yield Optimization functionality, these performances were increased to a level of around 4 sigma. Because of topology specific trade offs, the high partial yielding transit-frequency was decreased to around 4 sigma. The overall total design yield of the circuit for the new process technology was increased to 99.99% (4 sigma). Simulation effort for this task was 16 min.

WiCkeD Results



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