

Circuit & Application

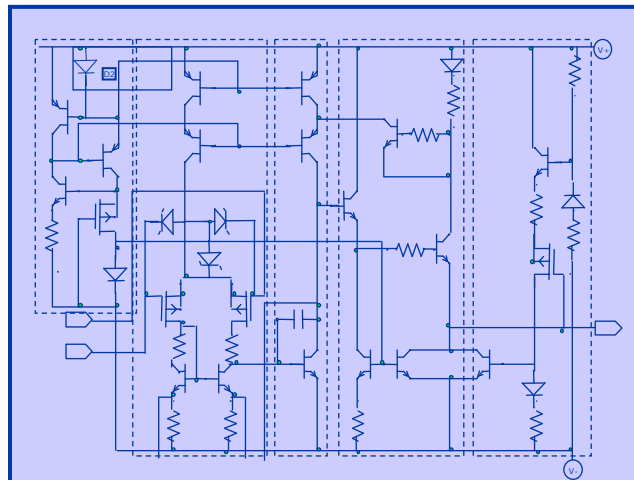
Operational Amplifier connected with biasing block generating all required bias voltages/currents. The circuit was designed for use in a Flash Memory. Process technology used was 500nm.

Problem Formulation and Goals

Particularly power consumption was too high and phase margin too low. In the required operating range the circuit did not work as specified, especially with respect to temperature and voltage. The yield of first silicon (done without WiCkED) was close to 0%.

Design Problems without WiCkED:

- ↘ Power consumption was too high.
- ↘ Phase Margin was too low.
- ↘ Design robustness was too low.
- ↘ First silicon yield was ~0%.



Solution using WiCkED

Step 1 — Adaptation of the component values

By adjusting the component values, internal constraints met their goals with respect to the saturation reserve and minimum area. Thus, functionality over the entire operating range was improved and robustness of the circuit increased.

Step 2 — Nominal Diagnosis

Utilizing WiCkED's visualization of the dependencies between component values and quality, the developers modified the circuit interactively.

Step 3 — Automatic Nominal Sizing

Devices were sized with WiCkED in a way that the circuit met the required specifications for the entire operating range.

Step 4 — Tolerance Analysis and Worst-Case Diagnosis

Tolerance Analysis quantified the influence of process variations on the circuit. Using this information together with Worst-Case Diagnosis the designers were able to adapt the components to maximize robustness versus the process variations.

Step 5 — Monte Carlo Analysis

Monte Carlo analysis validated the expected parametric yield the designers achieved with interactive design centering.

WiCkED Results

