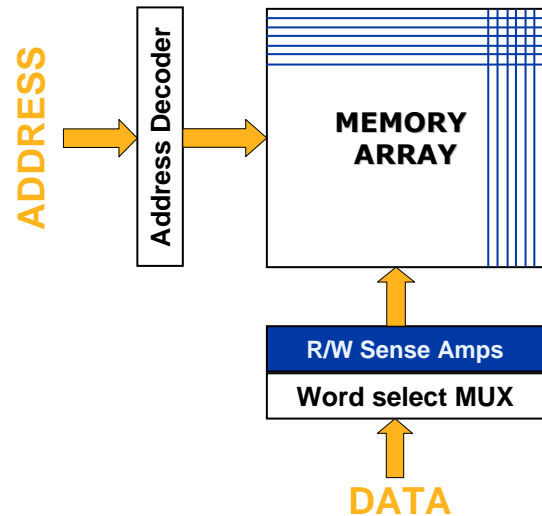


Circuit & Application

Highly sensitive sense-amps used for charge detection in SRAM memories. Such memories require 6 sigma design for each cell. Process technologies used were 180nm, 130nm, 90nm, 65nm.

Problem Formulation and Goals

Predicting and improving the design quality in terms of performance, yield and robustness in the range of 6 to 7 sigma are a central concern in designing sense-amplifiers for use in SRAM cells. Many sense-amplifiers are on one die and therefore the yield of each has to be very high. All units of one chip have to work in order to make the whole chip work. A single failing sense-amp means the whole memory fails hence yield loss.



Solution using WiCkED

Step 1 — Feasibility Optimization

Using automated structure recognition, sizing rules were detected and met automatically in order to find a feasible solution as a starting point.

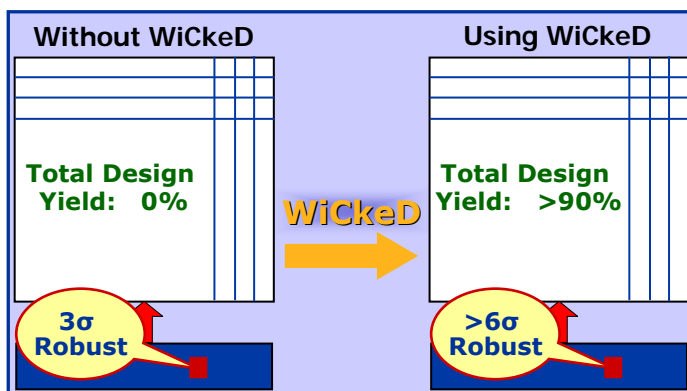
Step 2 — Nominal Optimization

Using WiCkED's DFM Optimization all circuit performance specifications were fulfilled. As a result, yield analyses showed increased robustness and yield. However, statistical optimization was still necessary to get to the desired level of 6 sigma and a design yield of 99.9997%.

Step 3 — Yield Optimization

Using WiCkED's Worst-Case Analysis the worst-case points were found. The worst-case point marks the region in the space of process parameters, where parametric faults are most likely to occur. Also, Mismatch Analysis showed the relevant mismatch pairs for the performances. Using WiCkED's Yield Optimization functionality the worst-case performances were increased to a level of about 6 sigma and the existing mismatch effects were reduced to an acceptable minimum.

WiCkED Results



- WiCkED achieved 6 sigma robustness for each cell, starting from a conventional process corner optimized level of 3 sigma.
- After WiCkED optimization the read-amplification sensitivity to the process variations was dramatically reduced.
- The SRAM-cells were sized to produce a total design yield of more than 90% as compared to a yield of close to 0% when using conventional process corner optimization.