

Circuit & Application

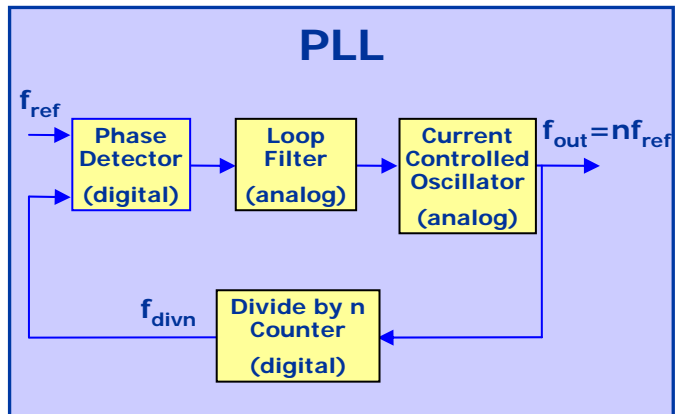
The circuit is a phase locked loop with the following Performance criteria: PLL lock time, attenuation factor and natural frequency. Process technology used was 130nm.

Problem Formulation and Goals

The hierarchical simulation was used, but serious compute resource problems arose as well as data inconsistency.

Design Problems without WiCkeD:

- Required memory too large: 2900 MB
- Simulation time too high: 191 min
- Data consistency not guaranteed.



Solution using WiCkeD

It was necessary to increase the resource efficiency. Using WiCkeD, the problem was solved within three design steps:

Step 1 – Improvement of sequence control

By using WiCkeD's database the consistency of data was guaranteed. The hierarchical simulation was correctly controlled with the help of WiCkeD's script control. The memory requirement was halved.

Step 2 – Improvement of Modeling

By shifting the borders from analog modeling to digital modeling within the single blocks, it was possible to reduce the simulation time. Also, the memory consumption was further decreased.

Step 3 – Improvement of feature extraction

The frequency of a rectangular signal was extracted by just reading the times of the rising slope. Therefore, the amount of data was reduced which reduced the memory consumption.

WiCkeD Results

