
Special Session:
DFM/DFY Design for Manufacturability and Yield –
influence of process variations in digital, analog and
mixed-signal circuit design.

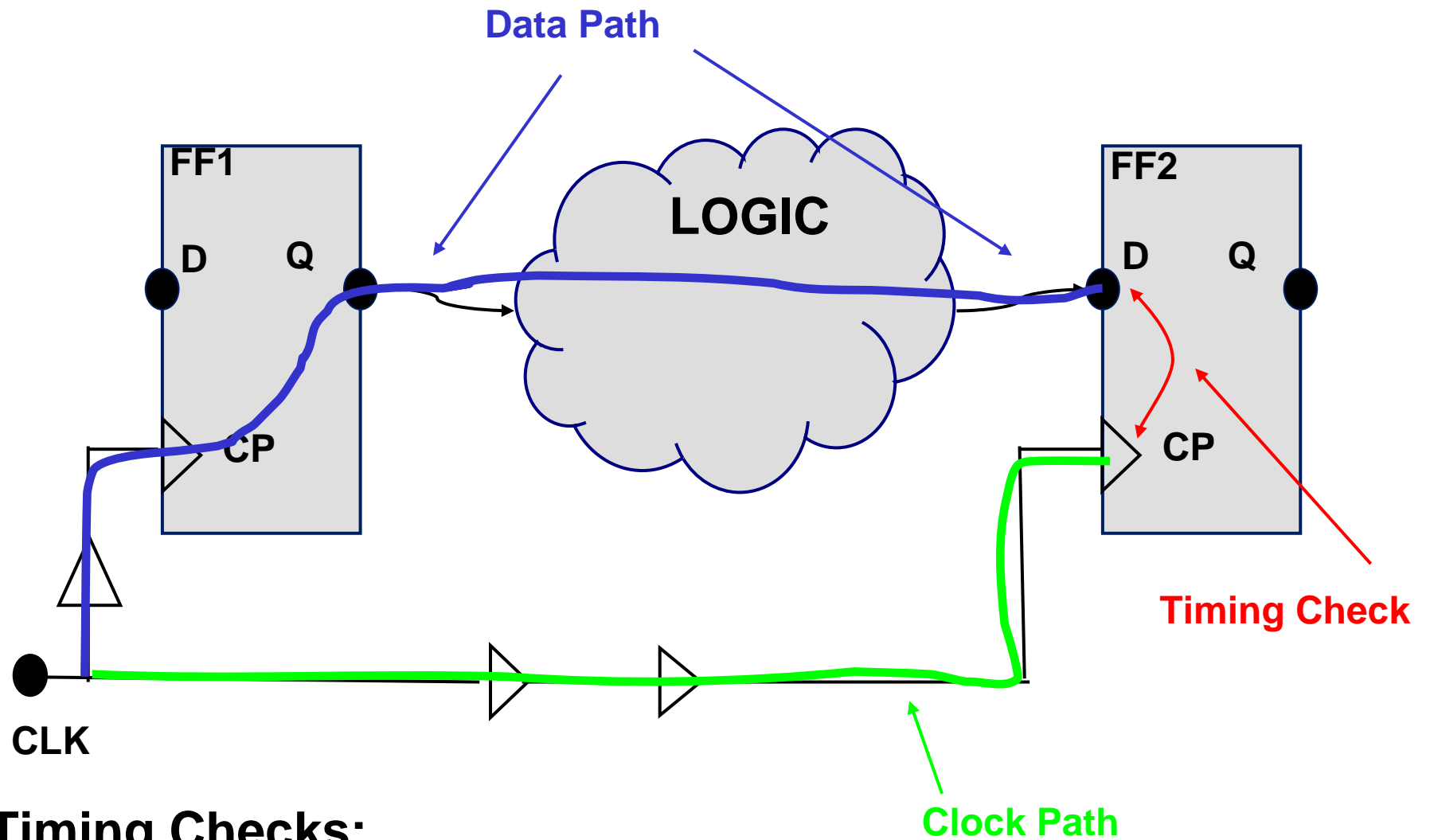
Statistical Design for Digital Circuits:
Statistical Static Timing Analysis (SSTA)

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Outline

- **Motivation**
- **Key Concepts and Challenges**
 - **Statistical Cell Delay Modeling**
 - **Statistical Timing Propagation**
- **Design Flow Integration and Outlook**

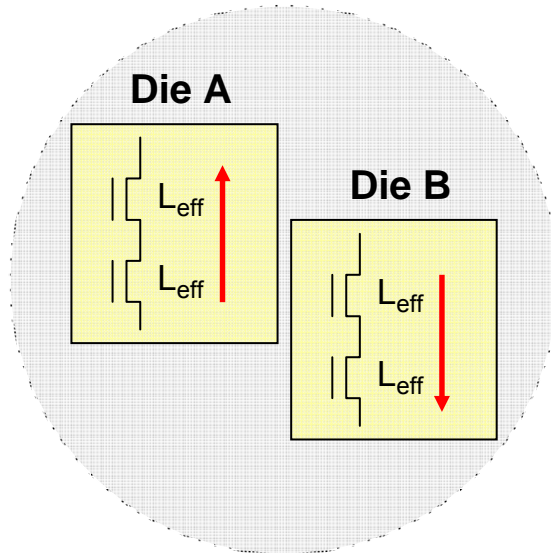
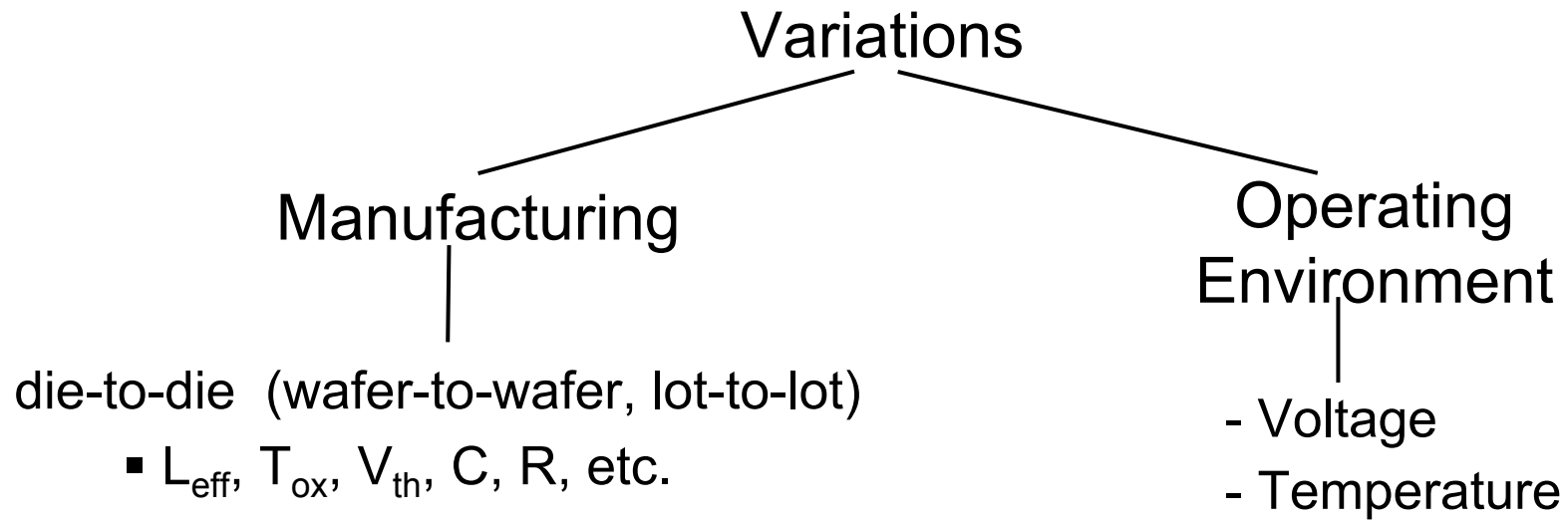
STA Basics



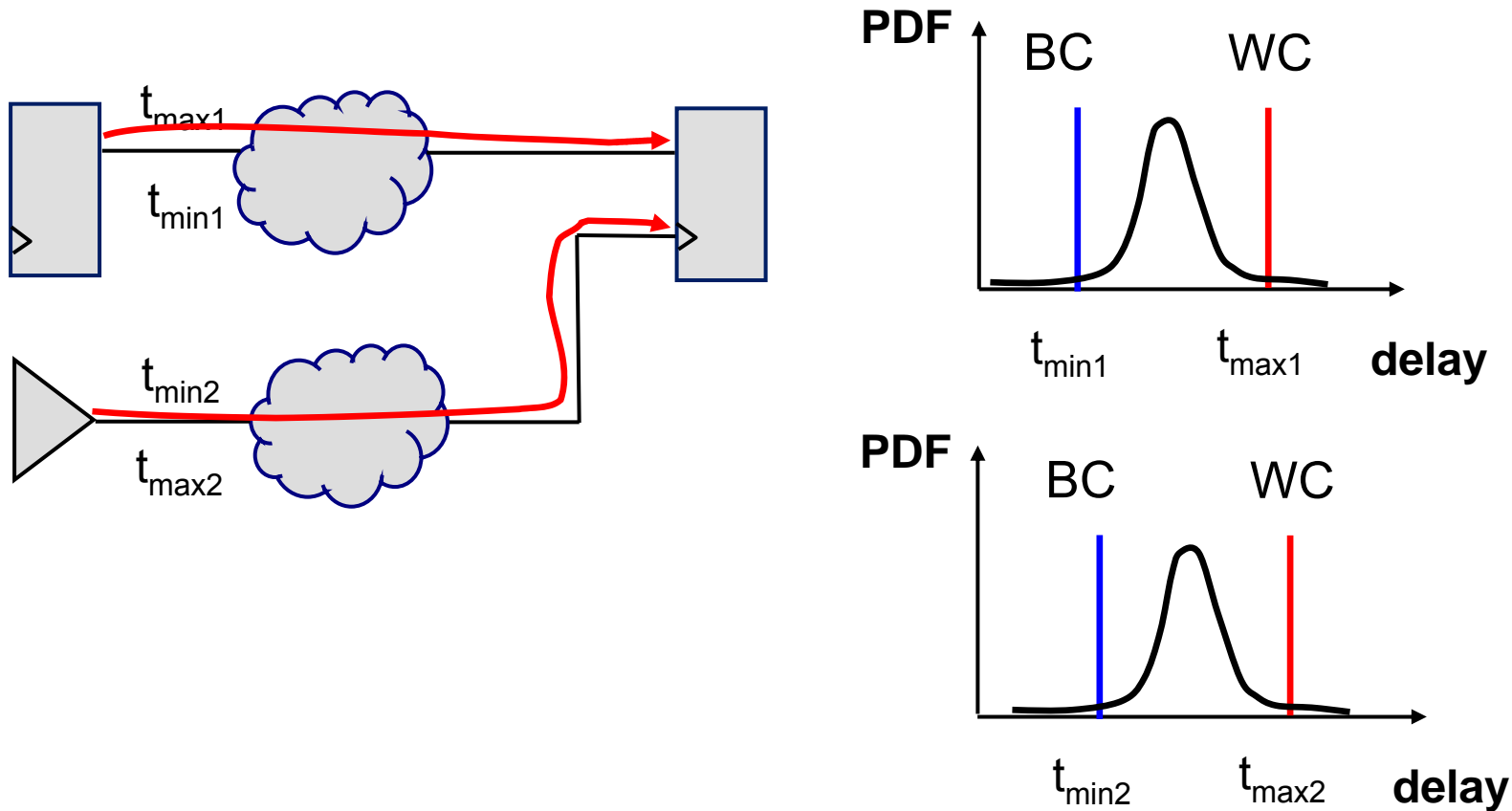
Timing Checks:

- Setup time check
- Hold time check

Traditional Variation Sources

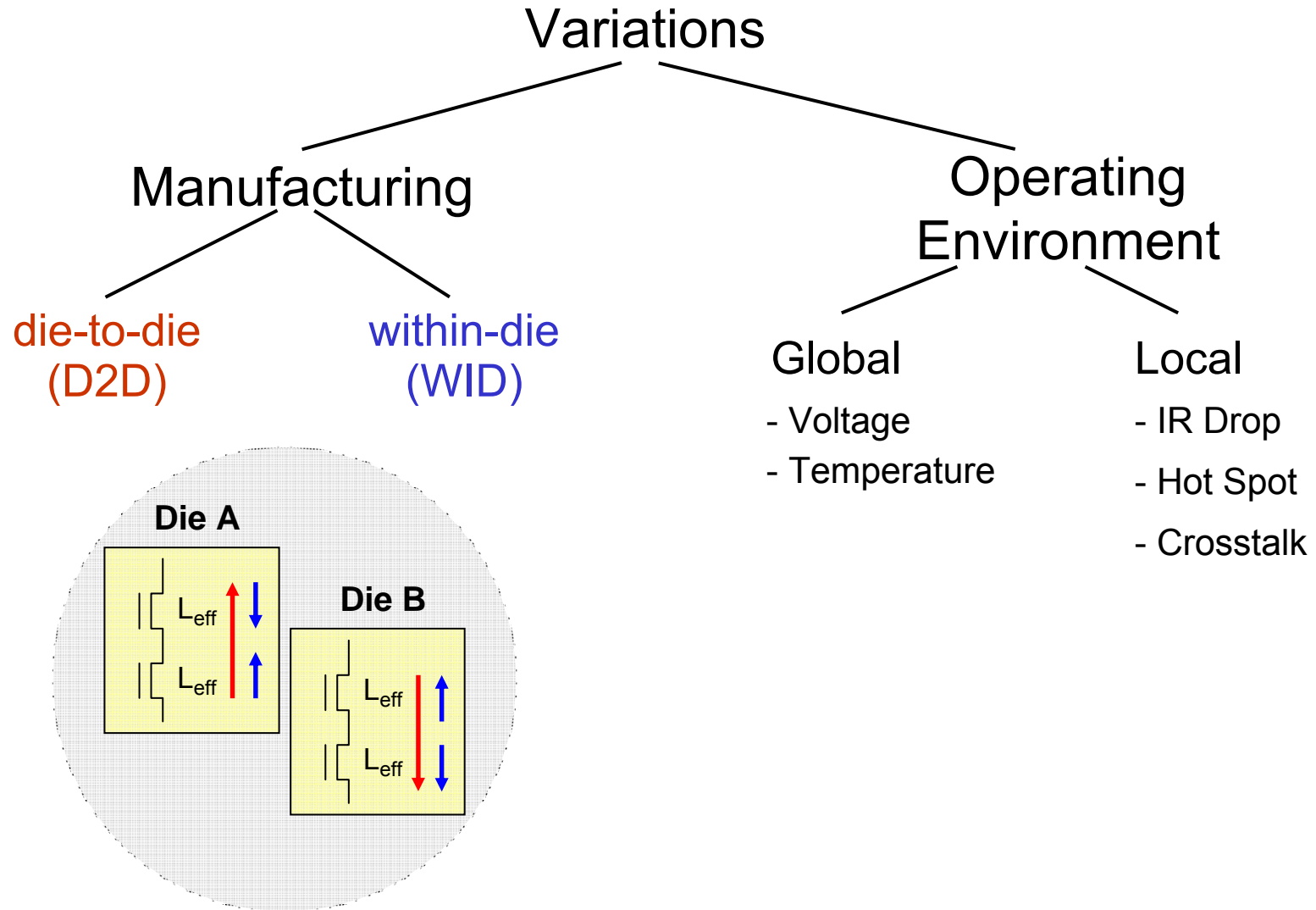


Corner-Based Static Timing Analysis



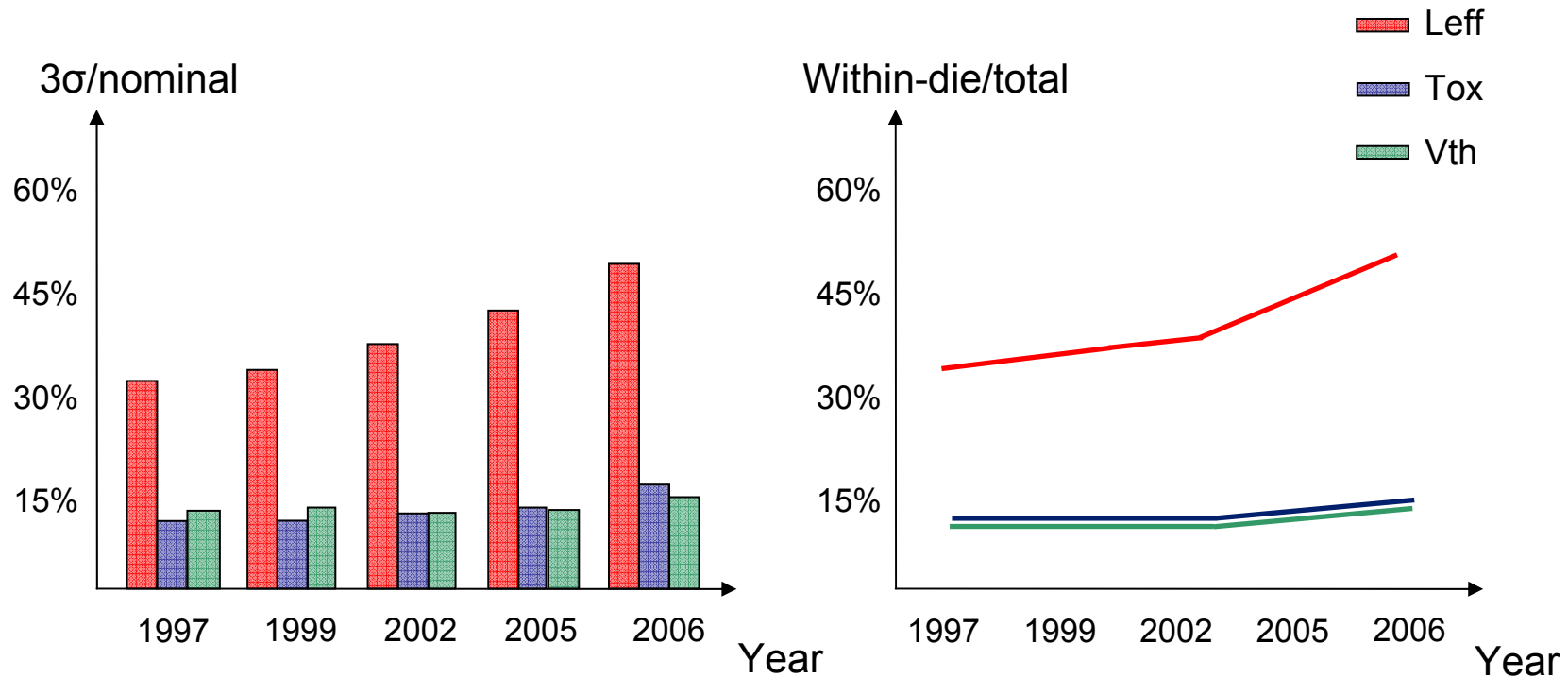
- **Longest paths:** worst case (WC) operating conditions (Setup)
- **Shortest paths:** best case (BC) operating conditions (Hold)

Variation Sources Today



Variation Trends

- Process variations continue to increase
- Within-die variations become more significant

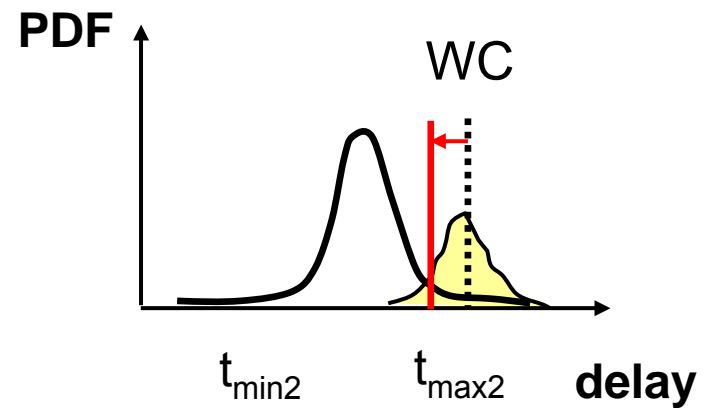
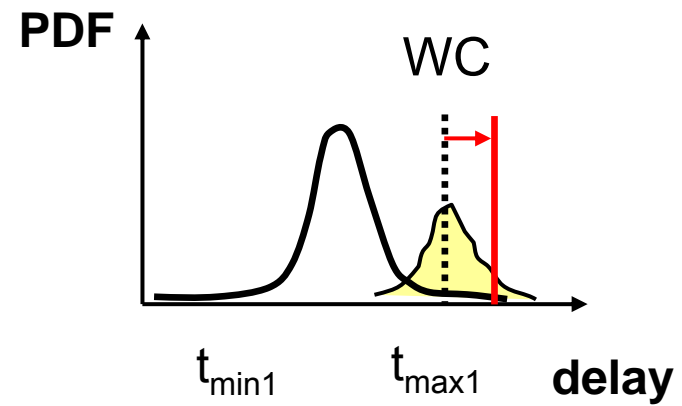
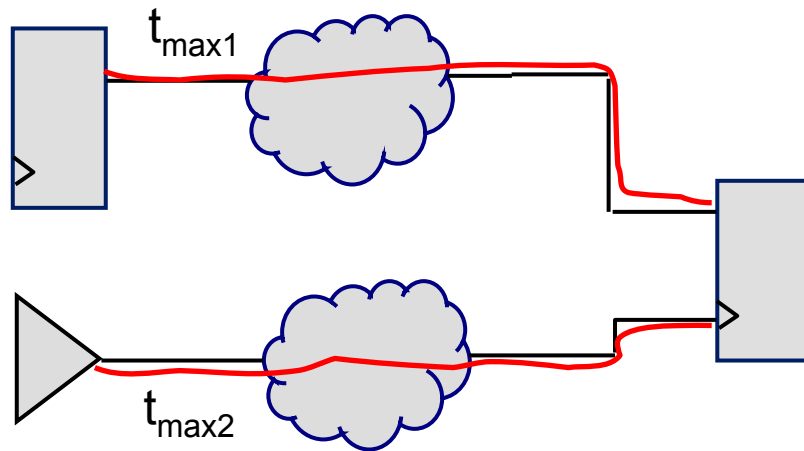


3σ parameter total variation relative to nominal value

Percentage of total variation accounted for by within-die variations

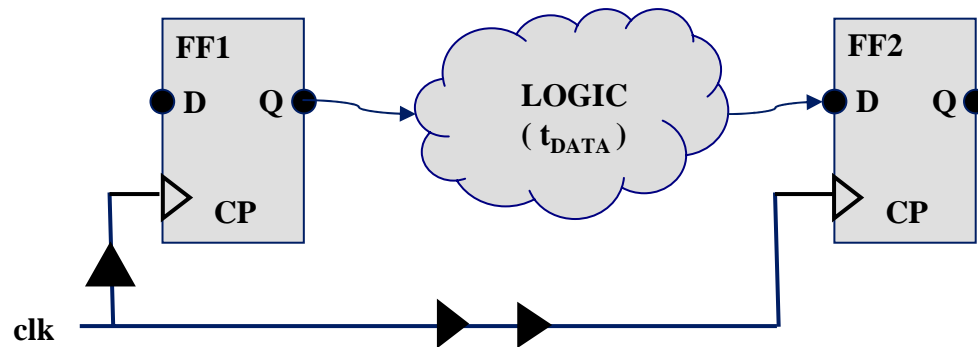
Within-Die Effects

- Within-die variations can affect the delay of paths differently
- e.g. data path becomes slower / clock path becomes faster



STA – Dealing with variations

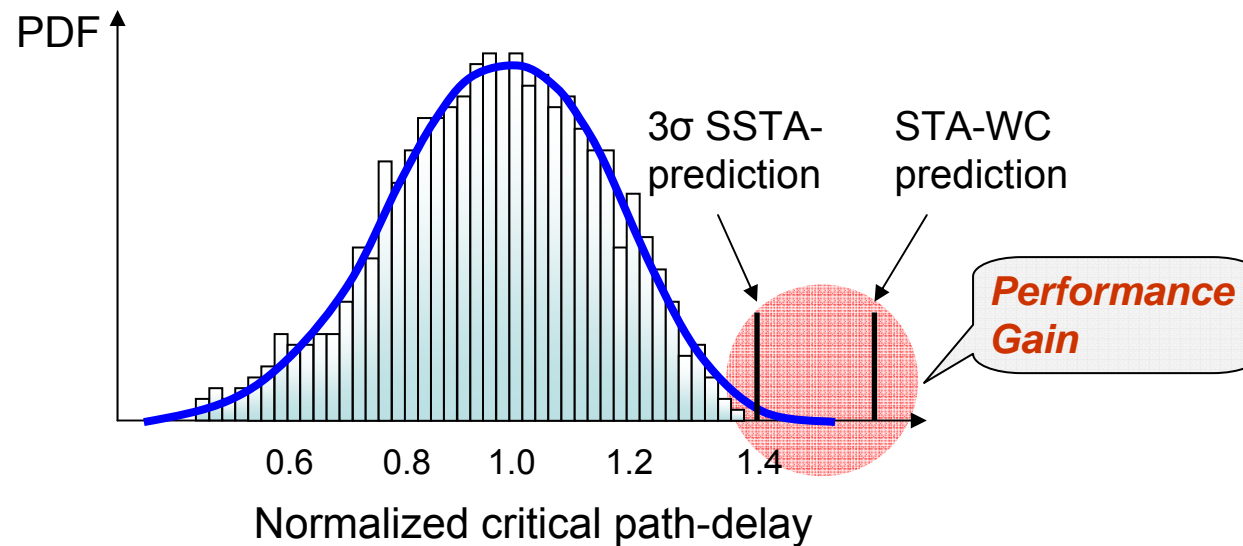
- Corner-Based Design (BC / WC):
all timing values are scaled



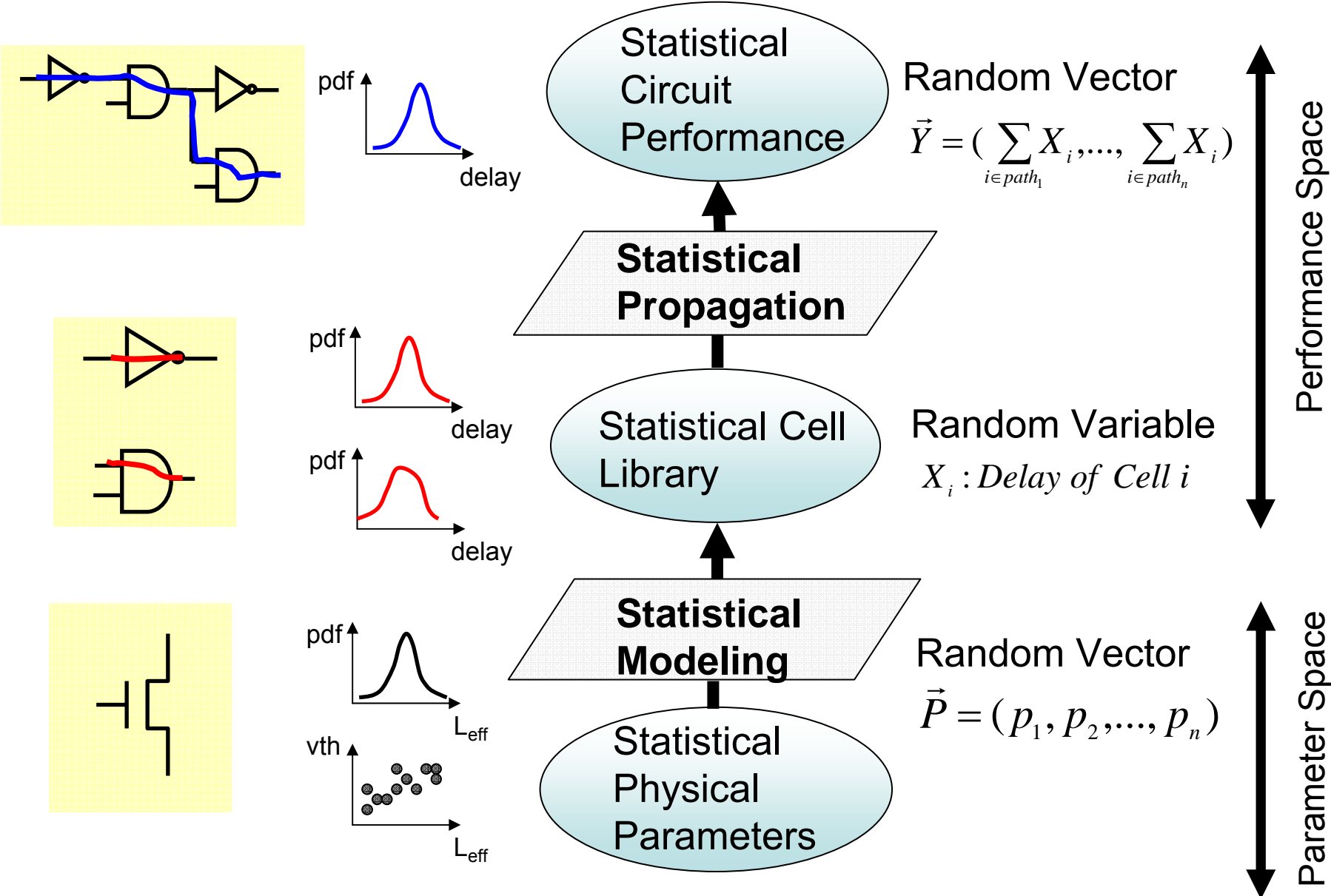
- Increase number of corners
- OCV-factor (on-chip variation)
- Statistical STA

Advantages of SSTA

- Proper consideration of statistical variations instead of performance loss due to excessive „guardbanding“
- Tradeoff between performance and yield

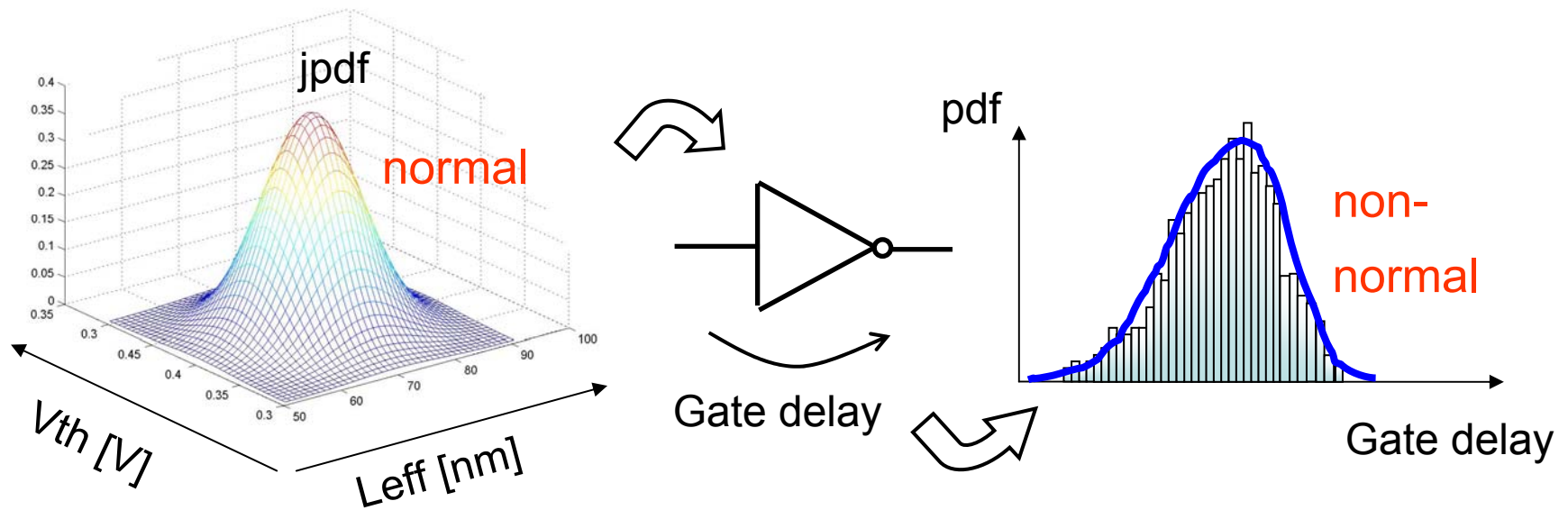


Basic Flow of SSTA



Key Problem in Performance Space

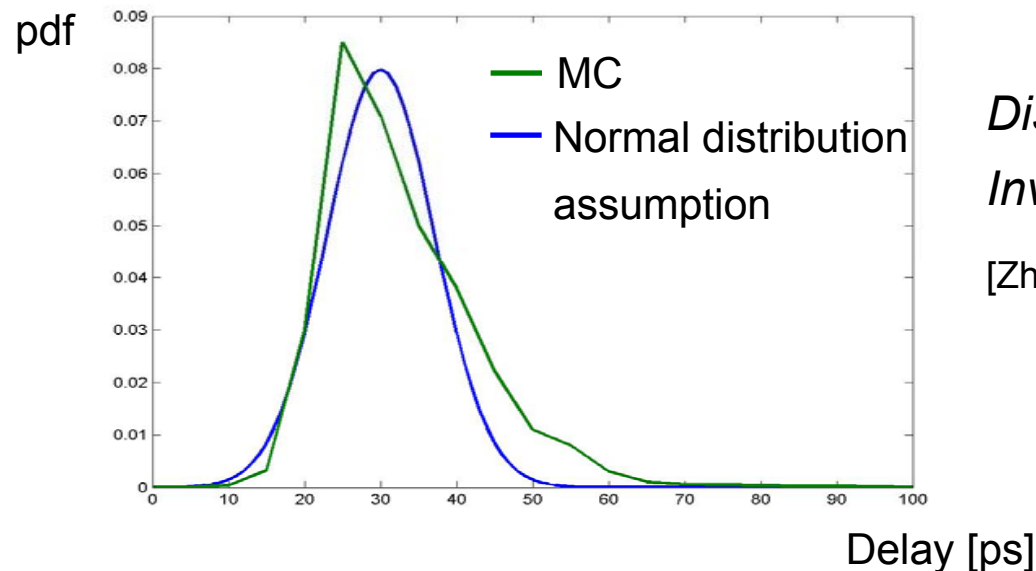
- Process parameters can be assumed to be normal
- BUT: Delay as a nonlinear function of normal distributed process parameters is NOT normal



- Normal distribution of gate delay only valid for small parameter variations

The normal distribution assumption

- Most SSTA algorithms rely on normal distributed gate delay
 - + distribution is captured by mean μ and sigma σ
 - + operations on random variables become easy
- inaccurate for large process parameter variations



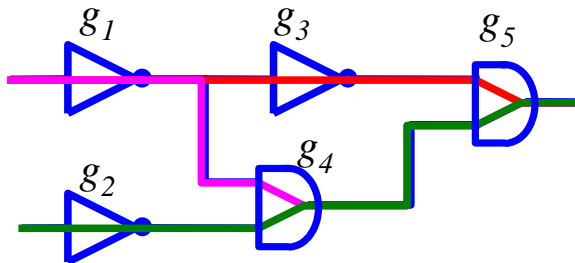
*Distributions of
Inverter Delay*

[Zhang et al., DAC 2005]

- Higher order models start to appear

Path- and block-based approaches

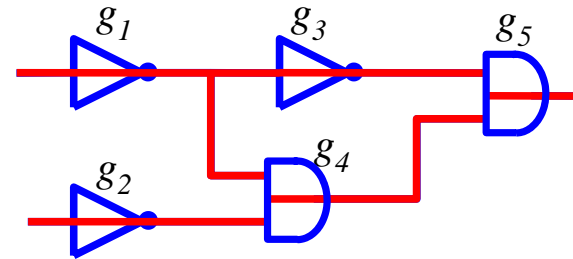
Path-based



- Enumerate all combinational paths $i = 1 \dots n$
- For each path i : determine PDF of path delay d_i
- Distribution of circuit delay d :

$$d = \max(d_1, d_2, \dots, d_n)$$

Block-based



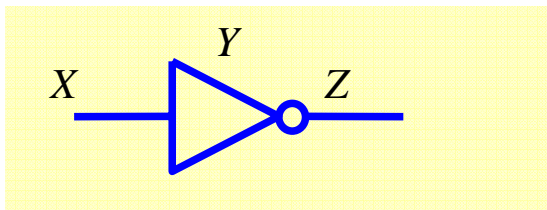
- Start at PIs, proceed in levelized fashion to POs / FF inputs o_i
- For each gate g_i : if PDFs of all inputs are known, determine PDF of output arrival time t_{out}
- Distribution of circuit delay d :

$$d = \max(t_{out}(o_1), t_{out}(o_2), \dots, t_{out}(o_n))$$

Propagation of Random Variables

- Two basic operations for propagating random variables:

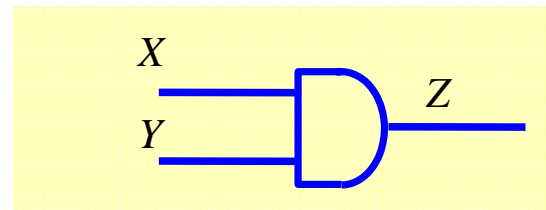
Sum:



$$Z = X + Y$$

$$F_Z(z) = \int_{-\infty}^{\infty} \left(\int_{-\infty}^{z-y} \underline{f_{X,Y}}(x, y) dx \right) dy$$

Maximum:



$$Z = \max(X, Y)$$

$$F_Z(z) = \int_{-\infty}^z \left(\int_{-\infty}^z \underline{f_{X,Y}}(x, y) dx \right) dy$$

- sum operation simple in case of joint-normal density $f_{X,Y}$:

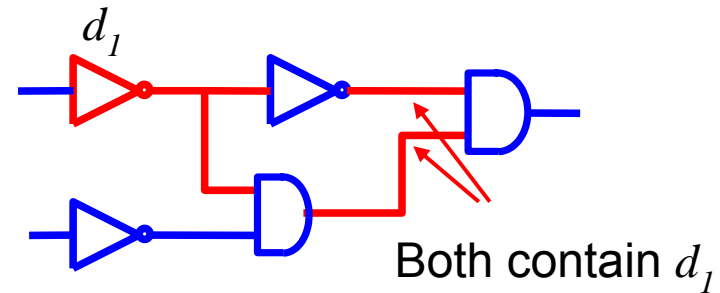
$$\mu(X + Y) = \mu(X) + \mu(Y)$$

$$\sigma^2(X + Y) = \sigma^2(X) + 2Cov(X, Y) + \sigma^2(Y)$$

- maximum operation introduces complexity in SSTA – solutions only presented for joint-normal density $f_{X,Y}$

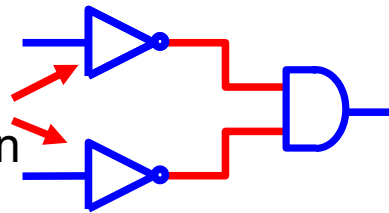
Sources of correlation

- Reconvergent paths (path sharing)



- Spatial correlations

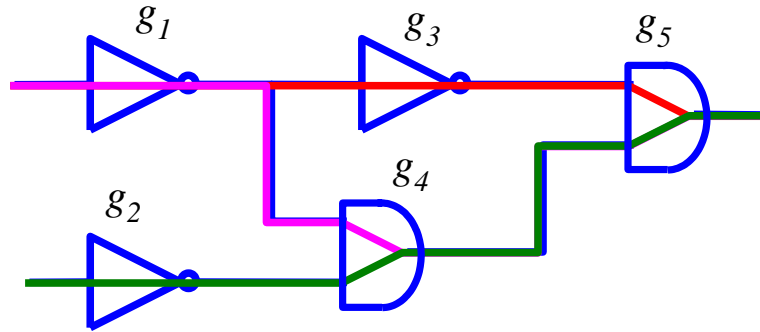
short distance
→ similar variation



- Correlated variables are not independent !

Correlation affects Circuit Yield

- PDF f_i for each path delay



path₁: g₁, g₃, g₅ with f_1
 path₂: g₁, g₄, g₅ with f_2
 path₃: g₂, g₄, g₅ with f_3

- Probability p_i , that delay of path_{*i*} meets timing target
 → Circuit Yield p , assuming:
 - independent path delays f_i :

$$p = \prod_i p_i$$
 - E.g. 100 paths with a probability each of 0.99:

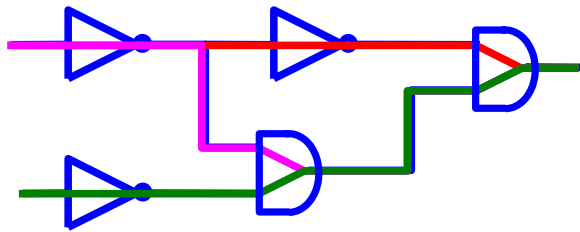
$$p = 0.99^{100} = 0.36 \text{ !!!}$$
 - perfectly correlated f_i :

$$p = \min(p_i)$$
 - E.g. 100 paths with a probability each of 0.99:

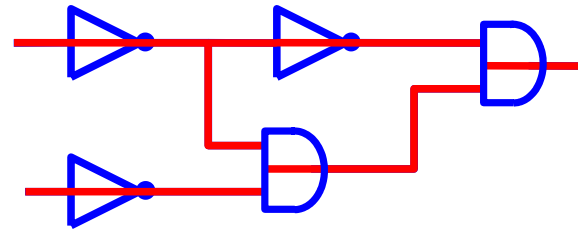
$$p = 0.99$$

Block-based vs. Path-based ...

Path-based

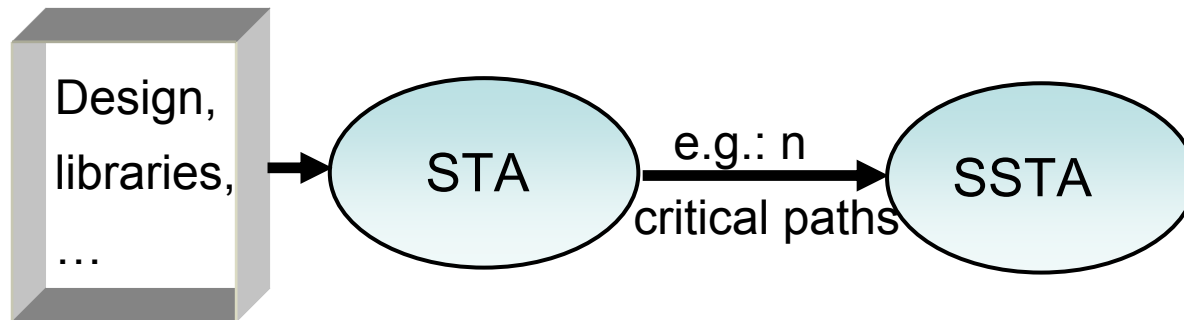


Block-based



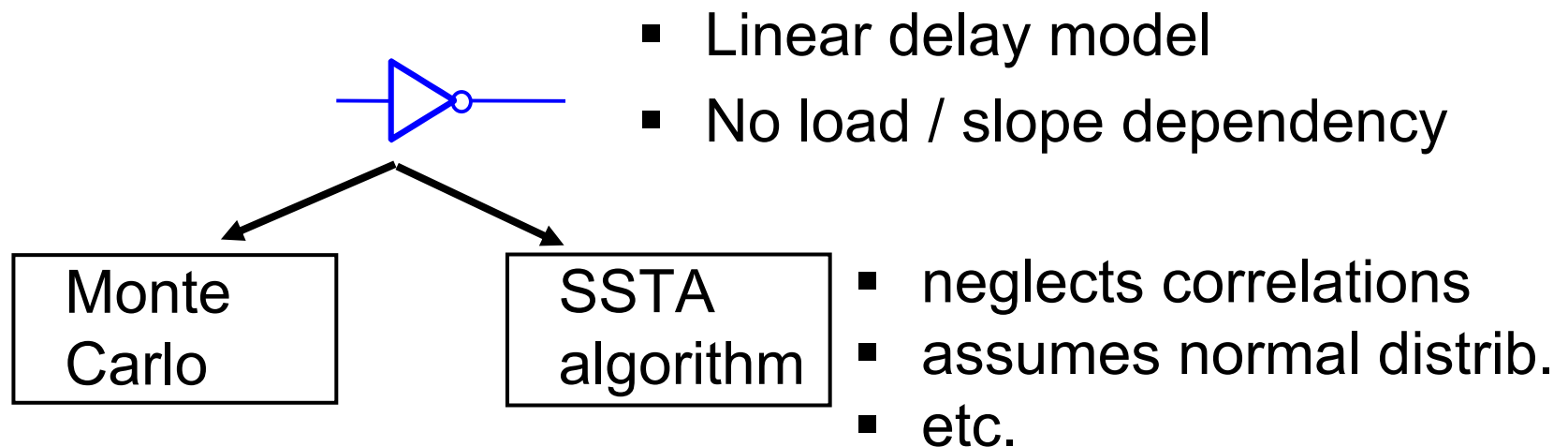
Accuracy	+	-
Run-Time	-	+
Applicability	?	?

Path-based: SSTA as postprocessor after STA



Verification of SSTA results

- Standard: Comparison to Monte Carlo
 - Results always look very good
 - But: inputs into MC matter!



Both results contain
delay model assumptions!

Statistical Design – Where are we?

- Is SSTA productionworthy yet?
 - IBM reports productive use of EinsTimer
 - Major EDA vendors announce SSTA features
 - Startups focus on SSTA

- BUT ...

Statistical Design – Where are we?

- Input data:
 - Trustworthy? Correlations?
 - IDM vs Foundry
- Basic approaches:
 - Path-based: preselection of paths risky
 - Block-based: accuracy unclear
- Delay modeling and propagation:
 - Load / slope consideration
 - Interconnect modeling
- Production testing:
 - At-speed testing required
 - How many paths to test?

Statistical Design – Where are we?

- Even with analysis, we're only at the beginning.
- Deterministic STA:
 - Research since 1982
 - Widespread industrial adoption since mid-90s
- Statistical analysis / optimization of analog circuits
 - Research since 1970s
 - Industrial adoption starting 1990s
 - Commercial availability since 2000s

- From statistical analysis to statistical optimization.

Acknowledgements

- Walter Schneider and the TUM SSTA team
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