

Common DFM-DFY contribution by austriamicrosystems and MunEDA at IEEE CICC 2006 - Experimental Verification of Simulation Based Yield Optimization for Power-On Reset Cells

Unterpremstätten-Austria / Munich-Germany - austriamicrosystems and MunEDA will contribute a common DFM-DFY paper presentation at the IEEE CICC Custom Integrated Circuit Conference 2006 (<http://www.ieee-cicc.org>) at September 10 - 13, 2006, in San Jose, California, USA. The contribution titles "Experimental Verification of Simulation Based Yield Optimization for Power-On Reset Cells" and will be given during the Session "Modeling and EDA" Challenges in Nano-CMOS. Authors of the contribution are Dr. Gerhard Rappitsch and Oliver Eisenberger from austriamicrosystems AG, Unterpremstätten, Austria as well as Dr. Bernd Obermeier, Andreas Ripp and Dr. Michael Pronath from MunEDA GmbH, Munich, Germany.

The session discusses and reviews modeling and EDA challenges in nano-scale CMOS technologies. The impact of variabilities on device and circuit performances will also be covered. Within the contribution the yield optimization of a analog circuits is performed by simulation based design centering. Critical parameters are determined from sensitivity analysis enabling yield enhancement by shifting of the production process. In a second step a new set of design parameters is computed maximizing the worst-case-distance. The simulated yield improvement for the initial design and the optimized design is verified by electrical wafer testing under varying production conditions.

Dr. Gerhard Rappitsch, Principal Engineer DFM (Design for Manufacturability) at austriamicrosystems, states: "A yield optimisation of an IP block was carried out using automated simulation based design centering and verification by experimental results. First, critical process parameters have been determined by sensitivity analysis allowing the improvement of production yield for the initial design by adjusting the PMOS threshold implant dose. In a second step a new set of design parameters was determined by simulation based yield optimisation where the goal was to keep the device area as small as possible and to maximize the worst-case-distance. The quality of the simulation results heavily relies on the accuracy of SPICE simulation models (Monte Carlo models) reflecting the global and local variations of the production process".

The yield analysis and optimization results were achieved using MunEDA's DFM-DFY tool WiCkeD and have been verified also on silicon.

About austriamicrosystems

austriamicrosystems' business unit Full Service Foundry has successfully positioned itself in the mixed signal foundry market offering well-established RF CMOS, High-Voltage CMOS, BiCMOS and SiGe-BiCMOS processes. With superior support during the design phase, high-end tools and experienced engineers, austriamicrosystems succeeds to be an attractive analog/mixed-signal foundry partner especially for fabless design houses. For more information, please visit www.austriamicrosystems.com.

About MunEDA

MunEDA provides leading EDA technology for analysis and optimization of yield and performance of analog, mixed-signal and digital designs. MunEDA's products and consulting enable customers to reduce the design times of their circuits and to maximize robustness and yield. MunEDA's solutions are in industrial use by leading semiconductor companies in the areas of communication, computer, memories, automotive, and consumer electronics. WiCkeD is a comprehensive and powerful software tool for interactive, manual, semi- and full automatic analysis, sizing, design centering and yield optimization of analog and mixed signal circuits. WiCkeD is marketed also under the trademark DesignMD®. For more information, please visit www.muneda.com.