

MunEDA User Group Meeting 2007

Dear MunEDA User,

We cordially invite you to come to our MunEDA User Group Meeting 2007 - MUGM07 - in Munich. Goal of the event is the intensive exchange of experience by industrial users of MunEDA's DFM-DFY software tools. We are very pleased to gain excellent speakers and contributions for this MunEDA User Group Meeting. Besides other contributions one main focus of the MunEDA User Group Meeting 2007 is the special topic:

Design Flow & Technology Integration of Nominal and Statistical Sizing Methods



Date: September 25-26th 2007

Location: Hilton Munich City
Rosenheimer Straße 15
81667 Munich - Germany



MunEDA User Group Meeting 2007 Agenda will contain contributions from:



and others ...

Presentation Topics of MUGM2007:

- Integration of Statistical Sizing Methods in Analog-Mixed-Signal-Flow
- Automatic Analog Circuit Synthesis using WiCkeD
- Robust and Reliable Analog Design for Automotive and Sensor Applications
- Memory - PLL Hierarchical Optimization Methodology Considering Jitter, Power and Locking Time
- Technology setup for WiCkeD in CMOS and BiCMOS Process for Automotive and Sensor Applications
- Optimization of I/O Macro Cells with WiCkeD
- Introduction of Analog IP Porting Flow Concept
- Automatic Flow for Library Cell Optimization
- Basics of Analog Circuit Modelling and Simulation
- Analysis and Optimization of a CMOS Mixer Circuit
- And more...

We are very looking forward to welcome you to our MunEDA User Group Meeting 2007 in Munich.

Andreas Ripp

Vice President Sales & Marketing

AND YOUR

MunEDA

TEAM

Dr. Michael Pronath

Vice President Products & Solutions

Register at: www.muneda.com/MunEDA-User-Group-Meeting

Participation for MUGM07 is free but early registration and accomodation is highly recommended because of co-located Munich Oktoberfest.

MunEDA User Group Meeting 2007 – Conference Program

Day 1 – Tuesday, September 25th, 2007

09.30 h - 10.00 h	Registration & Welcome Coffee
10.00 h - 10.30 h	Welcome & Whats new Andreas Ripp, VP Sales & Marketing, MunEDA GmbH
10.30 h - 11.00 h	Optimization of I/O Macro Cells with WiCkeD M. Mauthe, Senior Staff Engineer, Infineon AG / A. Hebenstreit, Staff Engineer, Infineon AG
11.00 h - 11.20 h	Coffee & Discussion Break
11.20 h - 11.50 h	Designflow Architecture and Integration of Statistical Sizing Methods in STMicroelectronics Non-Volatile-Memory (NVM) and Automotive Flow P. Daglio, NVM Mixed-Signal Design Flow Program Manager, STMicroelectronics
11.50 h - 12.20 h	Robust and Reliable Analog Design for Automotive and Sensor Applications by Combining Design Centering and SOA Techniques U. Sobe, ZMD AG / K.-H. Rooch, ZMD AG
12.20 h - 13.30 h	Lunch Break
13.30 h - 13.45 h	HOT-Topics J. Qiu, MunEDA GmbH
13.45 h - 14.15 h	MunEDA Tools and R&D-Roadmap F. Schenkel, VP Research & Development, MunEDA GmbH
14.15 h - 14.45 h	Automatic Analog Circuit Synthesis using WiCkeD X. Wang, Johann-Wolfgang Goethe Universität Frankfurt am Main
14.45 h - 15.00 h	Coffee & Discussion Break
15.00 h - 15.20 h	Integration of Statistical Sizing Methods in Infineon Analog-Mixed-Signal-Flow E. Hennig, CAD Staff Engineer, Infineon AG
15.20 h - 15.45 h	Analysis and Optimization of a CMOS Mixer Circuit R. Frevert, T. Markwirth, U. Knöchel and R. Jancke, Fraunhofer IIS EAS
From 15.45 h	Social Event: Transfer to MunEDA Event at Munich Oktoberfest

Day 2 – Wednesday, September 26th, 2007

09.00 h - 10.00 h	Speakers Breakfast
10.00 h - 10.30 h	PLL Hierarchical Optimization Methodology Considering Jitter, Power and Locking Time J. Zou, Qimonda AG / H. Gräß, D. Müller and U. Schlichtmann, Technische Universität München
10.30 h - 11.15 h	Preliminary Title: Basics of Analog Circuit Modelling and Simulation R. Sommer, TU Ilmenau / IMMS gGmbH
11.15 h - 11.30 h	Coffee & Discussion Break
11.30 h - 12.00 h	WiCkeD Circuit Optimization Examples: A) Optimization and Centering of the Basic Cells of SRAM Memories B) Performance and Yield Optimization of Sense Amplifier for Automotive Applications E. Raciti, CAD Engineer, STMicroelectronics
12.00 h - 12.30 h	Qualification of WiCkeD for the austriamicrosystems DFM-DFY design flow T. Mörth, Section Manager Design Support, austriamicrosystems AG
12.30 h - 13.30 h	Lunch Break
13.30 h - 14.00 h	Automatic Flow for Library Cell Optimization K. Singhal, Synopsys Inc. / T. Vogels, Senior Applications Engineer, MunEDA Inc.
14.00 h - 14.30 h	Technology Setup for WiCkeD in X-FAB CMOS and BiCMOS Process for Automotive and Sensor Applications V. Boos, IMMS gGmbH / H. Wald, X-Fab Semiconductor Foundries AG
14.30 h - 15.00 h	Coffee & Discussion Break
15.00 h - 15.45 h	Special Topics: - IP Porting - Local Variations (Analog & Digital) M. Pronath, VP Products & Solutions, MunEDA GmbH
15.45 h - 16.00 h	Wrap-up Discussion and End of Conference Andreas Ripp, VP Sales & Marketing, MunEDA GmbH
16.00 h - 16.30 h	Farewell Coffee & Discussion

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