



Automatic Analog IP Generation with **1Stone**[®]

**MunEDA User-Group-Meeting Europe 2009
Munich**

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IPGEN Rechte GmbH

- IP GEN Rechte GmbH founded in June 2006
- Registered office: Stuttgart
- Engineering office: Bochum, Dresden
- Product: **1Stone**[®] Family
- Partners & Customers:





Lead by Innovation



IP Provider

*DCP-IP Core for Data Converters
(D&R Best IP 2008 Award)*

EDA-Solutions

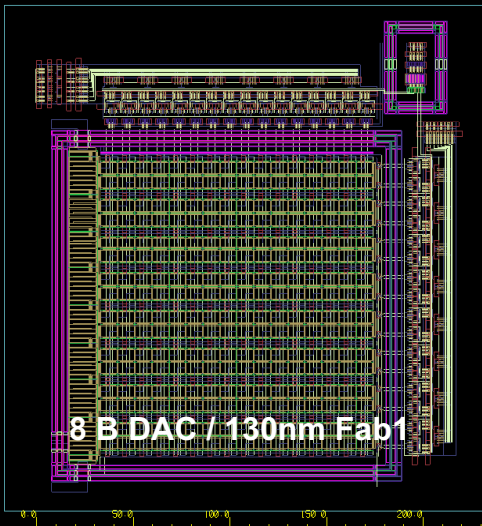
1Stone®

*GEM Methodology
(EDA Achievement Award 2006)*

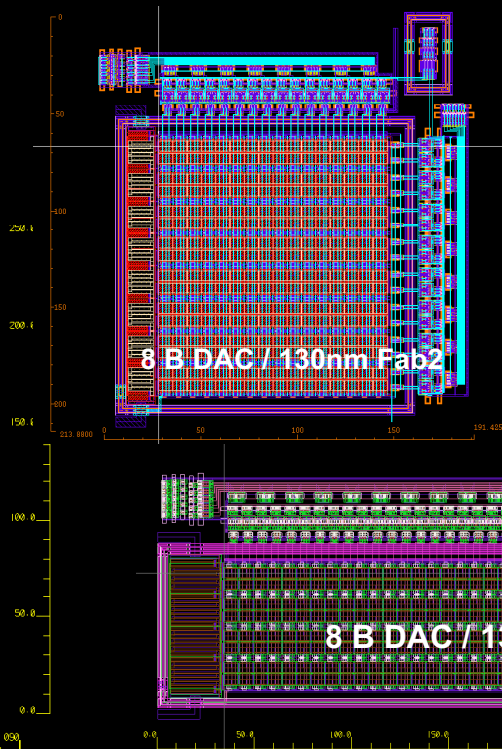


DCP-IP - Jumping across Borders

July 2003:
10 Person-Days for first Reuse
after 3 Years (0.35µm)



Oct 2003:
10 Person-Days to map
to Fab2 PDK
and 25% Area Reduction



Jan 2004:
8 Person-Hours for
new aspect ratio
and verification



1Stone/IPGEN Product

1Stone® : Engineering assistance for analog IP Design and Transfer

▪ Purpose:

Design rule aware IP creation/transformation for migration, technology transfer and reuse purpose (Focus analog/mixed/RF)

=> quality management (work flow planning and monitoring, high design efficiency, fast time to market, access to IP market, flexibility (process, application))

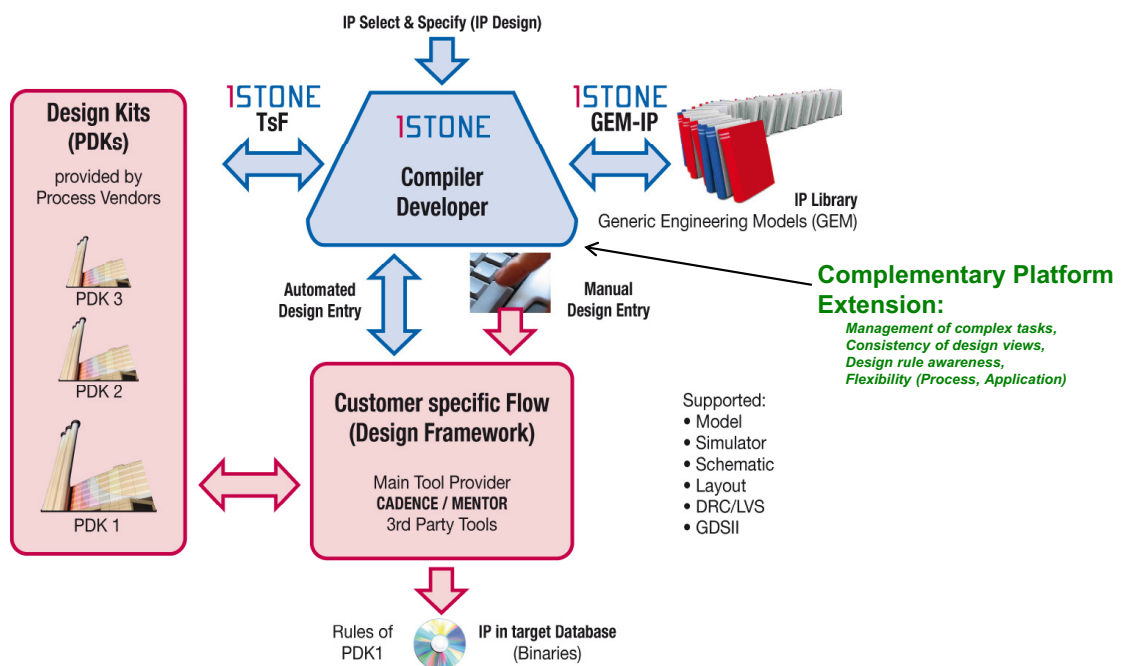
▪ Characteristics:

Full compatibility to Mentor & Cadence design & verification environment, Full compatibility to process design kits, DRC/LVS clean by construction



IC Design Flow with 1Stone® Product Family

IC Design flow with 1STONE Product Family



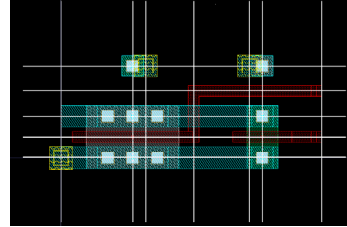


Alternative View on Circuit Design Process

- The Difference: Design and process related data is decoupled!!

- Basic Enablers:

- Device oriented virtual placing grid
- Symbolic parameterizable devices
- Portable device definitions
- Symbolic design rules
- Hierarchical design rules



Variable	Description
met1_layer	name of Metal1 layer in selected process
con_ndif_met1	name of the N-diffusion/Metal1 contact device
met2_spcmin	value for minimal metal2 spacing
poly_widthmin	value for minimal poly (poly1) width
pwel_ndif_minEnc	value for minimal enclosure for P-well over N-diffusion
mpoly_poly_r	value for poly (poly1) radius inside the metal1/poly contact
mpdif_m1m2	value for minimal center-center distance between metal1/metal2 and P-diffusion unconnected contact devices
poly_shRes	poly (poly1) sheet resistance [Ohm/square]
poly_poly2_areaCap	area capacity for a poly (poly1)/poly2 capacitor



Interpolating Flash ADC inside Cadence Framework

The screenshot displays the Cadence environment with a circuit schematic on the left, a module setup dialog for 'adc' on the right, and a console window at the bottom. The console shows the following text:

```

"Finished schematic of cell 'adc9b3 core_preamp' !"
Extracting "adc9b3 core_preamp schematic"
Starting ref+amp cell Placement...
ref+amp cell Placement done.
Starting ref+amp cell routing...
ref+amp cell Routing done.

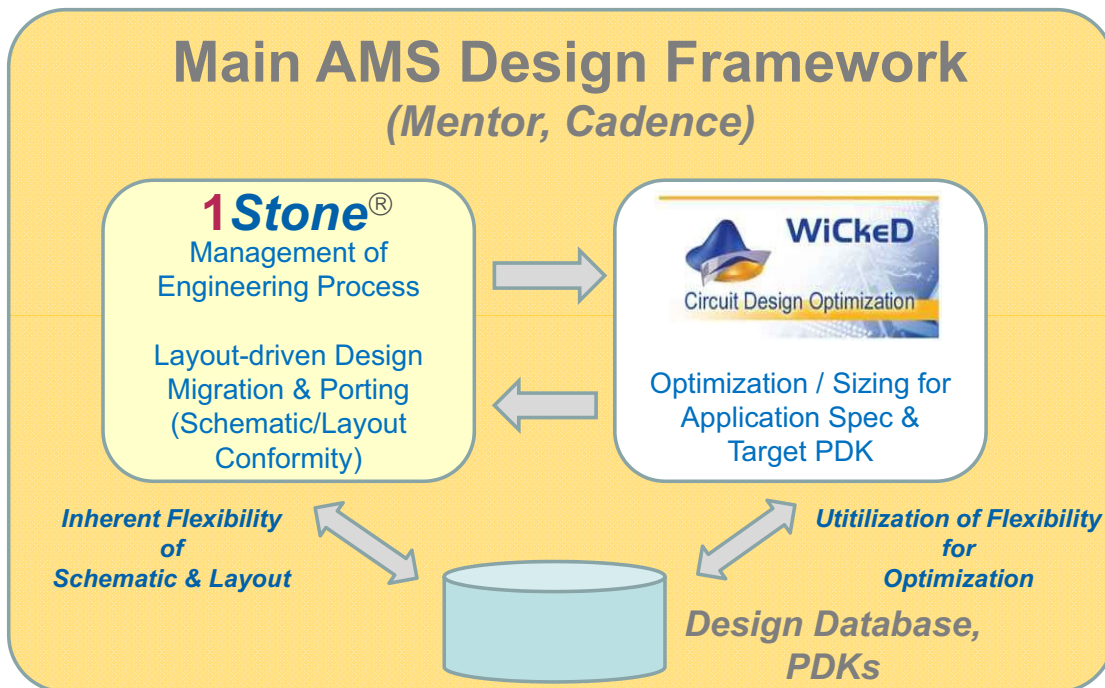
```

The 'adc - Module Setup' dialog has the following parameters:

Parameter	Value
cellName (string)	adc
resolution (int)	8
interpolation (int)	3
clkFreq (int)	50
layout (string)	false
schematic (string)	false
createSubCells (string)	false
powerPins (string)	true
crVerilog (string)	false



General Migration/Porting Flow



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Summary

Benefits of 1Stone[®] /IPGEN using GEM-based Descriptions:

- a significant enhancement of the design efficiency
- management of highly complex analog IC designs
- behavioral models tailored to the actual realization
- a high reliability of the designs by providing automated testbench-views
- a seamless documentation of the design steps for an existing reference design

Particular Features of this Design Approach are:

- the compatibility to given design flows, tools, and PDK's
- the remaining high degree of flexibility:
 - design parameters persist variable
 - designs persist portable between different PDK's and technology processes
- regularity seems to be one of the keys for accurate and reliable analog circuit design in nano-scale process technologies

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Experience



IP Catalog (~ 110 Person Years of Experience)

Analog (Silicon proved!)

- Potentiometer CMOS-DAC (4-15 bit, 50 kHz – 100 MHz)
- PWM-DAC (16-20 bit)
- Digital Potentiometer (on-chip digital calibration, accurate on-chip reference)
- Interpolating Flash ADC (6-10 bit, 20 – 100 MHz)
- SAR-ADC (6-12 bit)
- Comparators
- High Speed Buffer (for high loads: 20pF, 100 Ohm)
- Integer N PLL's (different concepts, integrated VCO)
- RF: LNA, Mixer, Coils (up to 6 GHz)
- Accurate Biasing Network for Transceivers
- Analog Signal Generators
- Actual Research: Adaptive TIQ/QVC Giga sample ADC (5 – 8 bit)



IP Catalog (~ 110 Person Years of Experience)

Digital (Silicon proved !)

- Memories: ROM, Dual Port RAM
- Standard Cell Catalog (fully characterized for digital work flow)
- Low Power Asynchronous Standard Cell Catalog
- IO cells including ESD protection
- Digital Pattern Generator Generators (extended to analog by using a DAC)
- Built-in-Self-Test Platform for Analog IP's

- Concepts (partly implemented): adder architectures, fixed-point multiplier, floating point multiplier (IEEE 754), barrel shifter



Higher performance using 1Stone®

Block	Effort Estimation			Performance	
	Today	1Stone first	1Stone reuse	1Stone	Comment
OTA (automotive)	2.5 PW	2 PW	0.4 PW	Equal or reduced power consumption	Optimization loop on layout level ,reference layout based design,architecture fixed Devices: 93 Paths: 650
Bandgap (different voltage domains, automotive)	5PW	4PW	1PW		Schematics and Floorplan available Devices: 300 Paths: 1700
Clock and Data Recovery-PLL	8PW	6PW	1 PM	Superior Lock-In (70 UI), 65nm, >30% reduced power (0.6mW @ 1V)	Optimization loop on layout level ,reference layout based design, architecture fixed, Accurate consideration of RF-parasitics Devices: ~ 300
Biassing Circuit	2 PM	2 PM* *configurable	0.25 PM	Floorplanning optimized for Matching 1-200 current sources (N or P driven), lout 20µA – 1mA, 130nm, 65nm	Algorithmic placement of distributed unity transistors for specified no. of currents, sample design reference available Devices: ~ 20 – 2000 (Spec dependent)
Biassing Circuit Extended	4 PM	1 PM* (reuse of biasing 1) *configurable	0.25 PM	Floorplanning optimized for Matching Digital programmable outputs	Algorithmic placement of distributed unity transistors for specified no. of currents, control bus Devices: ~ 20 – 2000 (Spec dependent)
DAC	12 PM	6 PM *configurable	1 PM	Linearity Gain: + 2-3 Bit Power Saving: > 50 % Area: > 50% Resolution: 4 -16 Bit (configurable)	Tailored resistors, speed trimming, algorithmic averaging Devices: ~ 3000 (8 Bit), ~ 20000 (12 Bit)
Flash ADC	12 PM	7 PM *configurable	1 PM	Optimized operating speed, Resolution 6-10 Bit (configurable) > 30% power reduction	Dynamic Performance: Tradeoff complexity vs. clock-rate Devices: ~ 30000 (9 Bit), ~60000 (10 Bit)

PW: person weeks

PM: person months

*Devices: Transistors, Resistors, Capacitors

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Some related Publications (1/2)

- R. Wittmann, W. Schardein, B. J. Hosticka, G. Burbach, J. Arndt, "Trimless high precision ratioed resistors in D/A- and A/D converters," IEEE J. Solid-State Circuits, vol. 30, no. 8, pp. 935-939, Aug. 1995
- R. Wittmann, D. Bierbaum, W. Schardein, E. Matei, "A parameterizable and process retargetable high speed DAC for digital radio applications", 12th Annual IEEE 1999 International ASIC/SOC Conference, Washington, Sept. 1999
- D. Bierbaum, R. Wittmann, M. Buchmann, M. Darianian, "A 2k high speed CMOS embedded dual port SRAM using an advanced generator concept", Forschungsreport "Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen", pp. 221-226, VDE Verlag, Feb. 2000
- R. Wittmann, W. Schardein, D. Bierbaum, M. Darianian, "SOC-driven design methodology for full custom high performance mixed-signal designs," 13th Annual IEEE 2000 Int. ASIC/SOC Conference, Proceedings, Washington, pp. 148-152, Sept. 2000
- W. Schardein, R. Wittmann, "A design environment using C for effective layout synthesis and development of reusable libraries", 1st IEEE International Conference on Circuits and Systems for Communication, ICCSC 2002, Proceedings, pp. 382-385, St. Petersburg, June 2002
- R. Wittmann, D. Bierbaum, P. Ruhanen, W. Schardein, M. Darianian, "A unified IP Design Platform for extremely flexible High Performance RF and AMS Macros using Standard Design Tools", System on Chip Design Languages (Extended Papers: Best of FDL'01 and HDLCon'01), ISBN 1-4020-7046-2, Kluwer Academic Publishers, Boston, June 2002
- R. Wittmann, J. Hartung, H.-J. Wassener, G. Tränkle, M. Schroter, "RF Design Technology for Highly Integrated Communication Systems", Proceedings DATE 03, Munich, 3-7 March 2003, pp. 842-847, IEEE Computer Society, ISBN 0-7695-1870-2
- EDA Achievement Award 2006, German edacentrum, Edaforum 2006, Berlin Nov. 2006
- P. Birrer, S. J. Chandrasekaran, R. Wittmann, „Partieller Layout Flow zur Generierung von Auswahltabellen für Bussysteme“, Proceedings, 1. GMM/GI/ITG – Fachtagung „Zuverlässigkeit und Entwurf“, 27-28. März 2007, München

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Some related Publications (2/2)

- P. Birrer, S. J. Chandrasekaran, R. Wittmann, „Partieller Layout Flow zur Generierung von Auswahltabellen für Bussysteme“, Proceedings, 1. GMM/GI/ITG – Fachtagung „Zuverlässigkeit und Entwurf“, 27-28.März 2007, München
- R. Wittmann, R. Kakerow, Ch. Münker, W. Schneider, P. Pirrer, „DETAILS: Neue Möglichkeiten für die Konzipierung und den Entwurf von höchstintegrierten Endgeräten mit besonderer Berücksichtigung der eingebetteten HF-IP Baugruppen“, Newsletter Edacentrum 01/07, S. 5-13, April 2007
- R. Wittmann, N. Nandra, J. Kunkel, M. Vanzi, J. Franca, H.-J. Wassener, Ch. Münker, "Life begins at 65 – Unless you are mixed-signal?", Proceedings DATE 07, Nice, 16-20 April 2007, pp. 936-941, IEEE Computer Society, ISBN 978-3-9810801-2-4
- R. Wittmann, D. Rosendahl, „Ausführbare Entwurfsablaufbeschreibungen für einen sicheren und effizienten Entwurfsablauf“, Silicon Saxony Workshop „Entwurf von integrierten Analog- / Mixed-Signal- / HF-Schaltungen“, 10. Mai 2007, Dresden
- J. Scheible, "Constraint-driven Design – Eine Wegskizze zum Designflow der nächsten Generation", Analog 08 GMM/ITG Fachtagung "Entwicklung von Analogschaltungen mit CAE-Methoden" 02-04 April 2008, Siegen
- M. Kosakowski, R. Wittmann, W. Schardein, "Statistical averaging based linearity optimization for resistor string DAC architectures in nanoscale processes", 21st Annual IEEE International SOC Conference, Newport Beach, Sept. 2008
- M. Kosakowski, R. Wittmann, W. Schardein, "Yield optimization to gain reliable and area efficient data-converters using nonideal nanoscale processes", 2. GMM/GI/ITG-Fachtagung "Zuverlässigkeit und Entwurf", Ingolstadt, Oct. 2008
- M. Kosakowski, R. Wittmann, W. Schardein, H.-J. Jentschel, "Yield prediction and optimization to gain accurate devices for analog design in nonideal nanoscale processes", 10th International Workshop on Symbolic and Numerical Methods, Modeling and Applications to Circuit Design (SM²ACD '08), Erfurt, Oct. 2008



Further information available at
www.ipgen.de