Automatic Flow for Library Cell Optimization with Synopsys HSpice® & MunEDA WiCkeD™

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MunEDA SYNOPSYS
Improve Design Performance and Yield

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Improve Design Performance and Yield

Nanometer Yield Limiters

- Functional Yield (DfM)
  - *Geometry distortion due to optical aberration*
  - *Opens and shorts due to defects (catastrophic faults)*
- Crosstalk failures (Signal integrity)
  - *Coupling of adjacent signals*
  - *Coupling through power grid and substrate*
- Static and dynamic IR drop
- Thermal variation
- Parametric Yield (DfY)
  - *Performance degradation due to variability during manufacturing*
  - *Chip functions but does not meet specifications*
- Jitter and phase noise
- Age dependent degradation (Reliability)
  - *Electromigration*
  - *NBTI, HCI, and gate oxide reliability*

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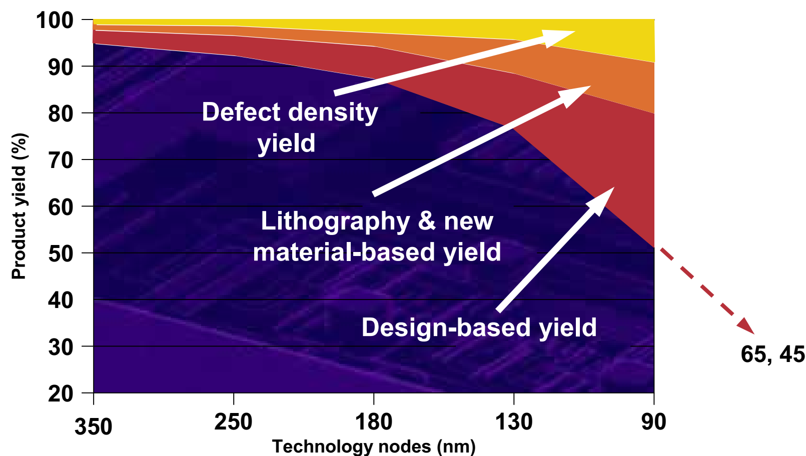
Parametric Variability will Dominate Yield Loss



Source: IBS Report

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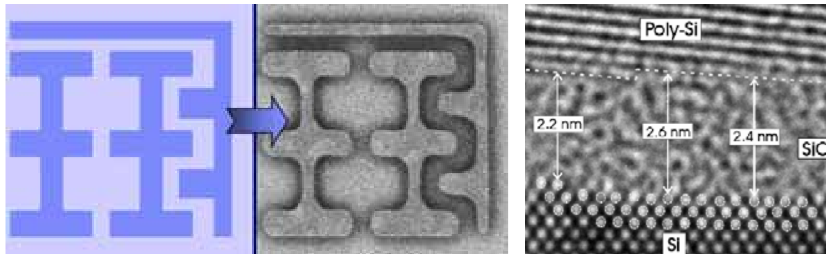
Examples of Variations



Litho Variation

Gate Oxide Variation

Source: IBM

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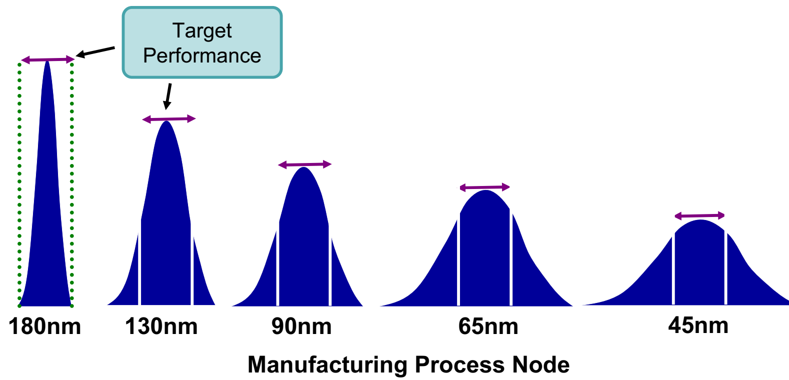
Paradox of Increasing Variation



Variations Increase For Each Process Node

Source: Synopsys

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Variability in Nanometer Technologies

- Higher fractional (%) variability with finer design rules & larger wafers (Table source ITRS)

L	250 nm	180 nm	130 nm	90 nm	65 nm	45 nm
Vt (mV)	450	400	330	300	280	200
σ_{Vt} (mV)	21	23	27	28	30	32
σ_{Vt}/Vt	4.7%	5.8%	8.2%	9.3%	10.7%	16%

- Lower voltages – less head room
- High speed & RF functions in CMOS
- Pressure to ramp products to volume & early profitability
- Mask costs $1M at 90nm, $2M at 65nm

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Parametric Variation Components

- Global (inter-die-variations)
  - *From chip to chip, across wafer, across lots*
  - *Influence all devices of a circuit the same way*
  - *Constant variance*
  - *For example:* t_{ox}
- Local (intra-die-variations)
  - *Influence all devices of a circuit differently*
  - *Variance depends on device area:* $\sigma^2_{local} \propto 1/W \cdot L$
  - *Increasingly important for digital*
  - *For example:* ΔL, v_{fb}
- Spatial
  - *Due to process and thermal gradients*
  - *Not important for small blocks*
- Proximity dependent
  - *Mostly systematic*

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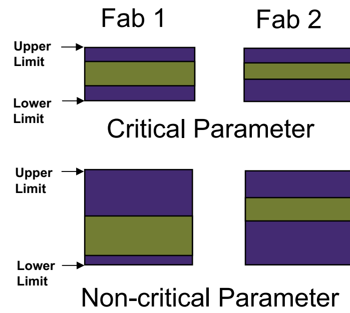
Variation Components (Fab)

- Fabs differ in equipment, geographic location, and process control policies
- Equipment capability is better in fabs that are constructed later and they have tighter distributions
- Even if the nominal or fast case are aligned between fabs, the spread is different
- Either use larger spreads or change pricing policy and charge a premium for the better fabs



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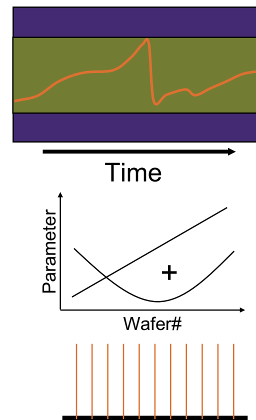
Variation Components (Lot, Wafer)

- Processes drift over time till
  - *Parameter reaches SPC limit*
  - *Equipment is cleaned*
  - *There is a yield bust*
- Latest fabs cost $2B and have much better monitoring and feedback-feedforward control
- Wafers in a lot tend to have a linear and/or quadratic gradient depending on their position



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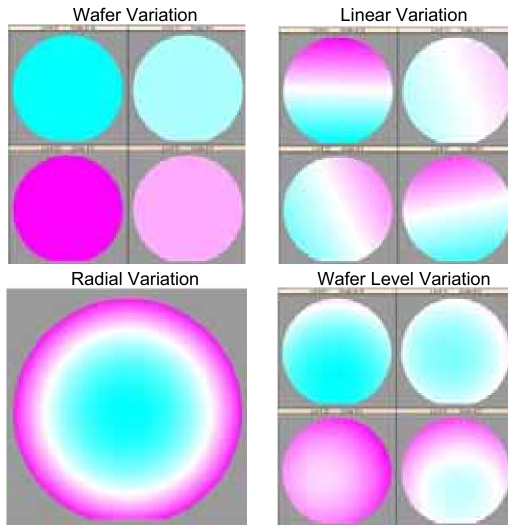
Variation Components (Wafer)



- Wafer variation comes from fab, lot, wafer processes
- Linear variation is due to materials and gas flow
- Radial variation is due to thermal and spin processes
- Wafer level variation is the sum of wafer, linear, and radial variation
- Affects mainly single-ended circuit performance measures like switching speed, gain, dynamic power etc.

Source: Synopsys

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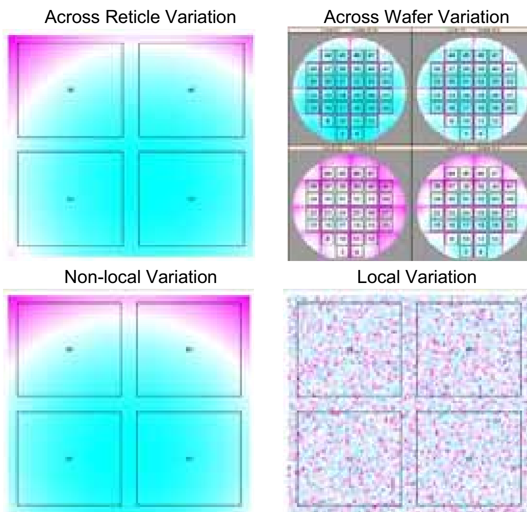
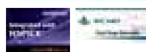
Variation Components (Reticle, Local)



- Reticle variation is due to photo processes
- Local variation comes from totally random microscopic processes. It affects mainly differential circuit performance measures like differential amplifier offset voltage, current mirrors, DACs, etc. Becoming important for digital design (30% of global variation at 130nm).
- Total parametric variation combines wafer, reticle, and local variations

Source: Synopsys



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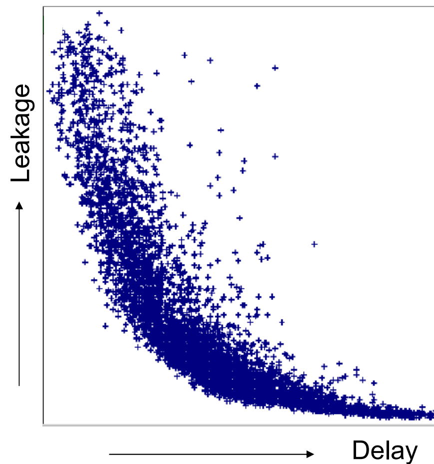
Influence of Process Variations on Digital Cells



Source: Intel

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Why Optimize Cell Libraries?

- Cells in the library are the basic building blocks of all ASICS
- Nanometer libraries have from 500 to 5,000 cells
- Library generation and creation is highly automated process
- Any improvement in performance and yield of the library cells has extremely high payoff as it is reflected in all future products that use the library
- Associated costs are amortized across the large numbers of instances of a cell on a given design and across multiple designs

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Optimization—An Example Setup

Optimization target

- Power—reduce leakage and dynamic power
  - *Given: Process variations, operating conditions*

Optimization constraints

- Minimal worsening of slew rate and delay
- Minimal increase in active area

Optimization variables

- Length and width of NMOS and PMOS transistors

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Synopsys/MunEDA — Automatic ASIC Library Optimization

- Automated optimization for ***performance*** and ***yield*** of digital and analog cell libraries
- Minimal and easy user interaction
  - **GUI to set technology/library specific geometric constraints and objectives**
  - **Cell optimization controlled by automatically generated customizable Tcl-scripts**
- Folds seamlessly into current digital cell layout and characterization flows and uses the same infrastructure/hardware

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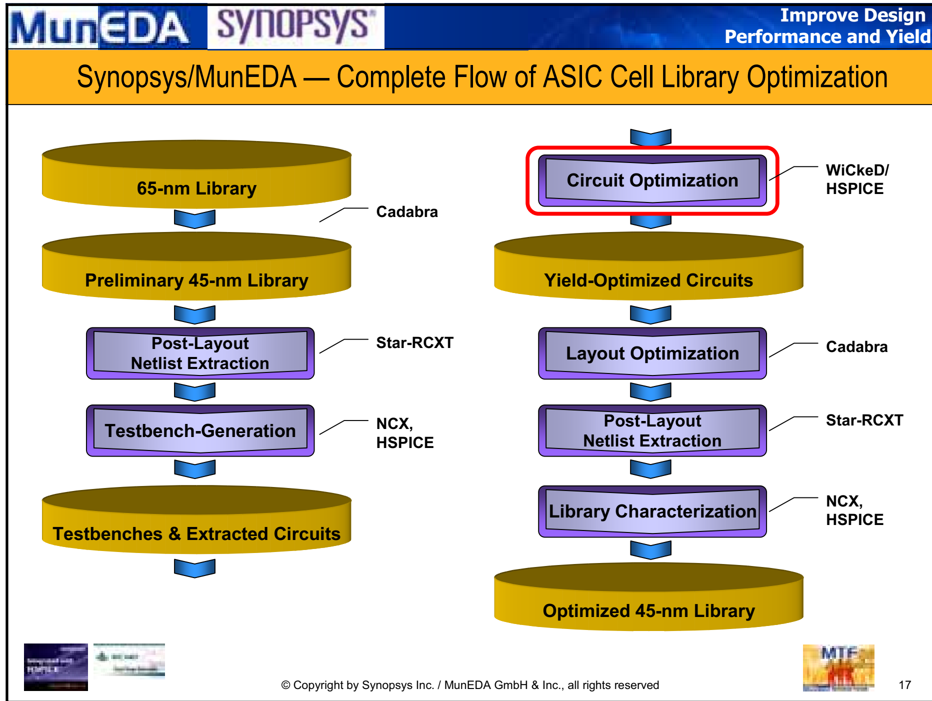
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Synopsys/MunEDA — Complete Flow of ASIC Cell Library Optimization
65-nm Library
Cadabra
Preliminary 45-nm Library
Post-Layout
Netlist Extraction
Star-RCXT
Testbench-Generation
NCX,
HSPICE
Testbenches & Extracted Circuits
Circuit Optimization
WiCkeD/
HSPICE
Yield-Optimized Circuits
Layout Optimization
Cadabra
Post-Layout
Netlist Extraction
Star-RCXT
Library Characterization
NCX,
HSPICE
Optimized 45-nm Library
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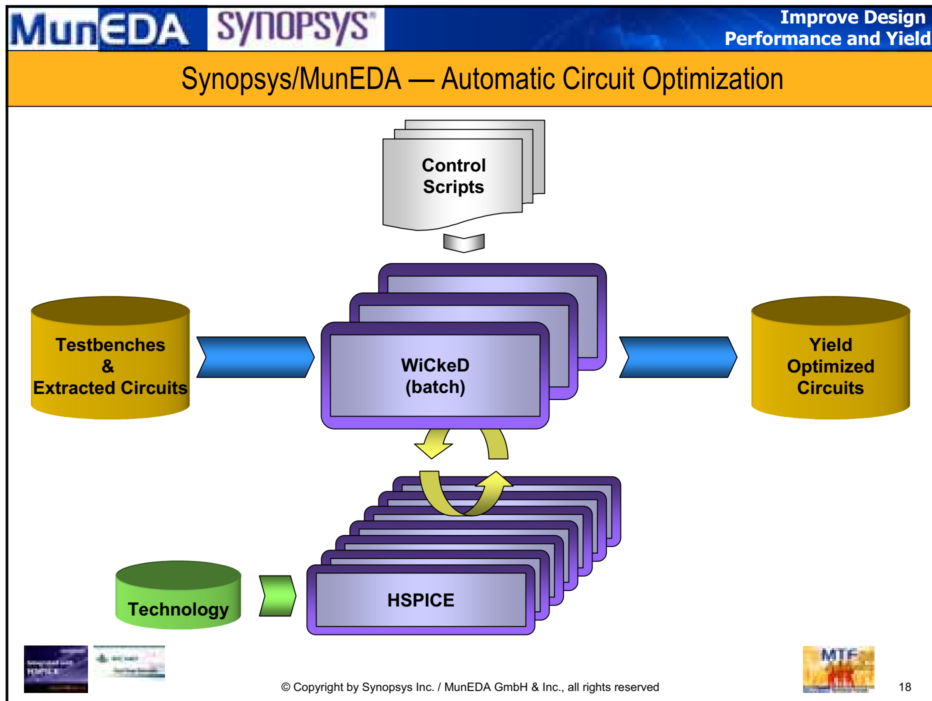
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Synopsys/MunEDA — Automatic Circuit Optimization
Control
Scripts
Testbenches
&
Extracted Circuits
WiCkeD
(batch)
Yield
Optimized
Circuits
Technology
HSPICE
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GUI-Concept of Setup Tool

File Options Help

Cells: invx2, bufx4, dly1x1, mx2x1, nand2x2, nand2x6, xnor2x2, aoi22x2, D_Flip_Flop, Scan_Enable_D

Technology Intent | Scripting

Design Parameters

	Lower Bound	Initial Value	Upper Bound
Transistor lengths	60 nm	60 nm	100 nm
Transistor widths	-30 %	+ 0%	+10 %

Apply

Operating Parameters

Name	Lower	Initial	Upper
Temp	-40 °	27 °	125 °
Cload	---	10 pF	---

Lower Bound	Initial Value	Upper Bound
-40 °	27 °	125 °

Apply Clear

Specifications/Constraints

Performance	Constraint	Lower Specification	Upper Specification
Leakage_Power		---	-20 %
Dynamic_Power		---	-20 %
Slew_Fall	+++	-5 %	---
Slew_Rise	+++	-5 %	---

Constraint — Lower Specification: ; Upper Specification: -20 %

Clear Apply

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GUI-Concept of Setup Tool

File Options Help

Cells: invx2, bufx4, dly1x1, mx2x1, nand2x2, nand2x6, xnor2x2, aoi22x2, D_Flip_Flop, Scan_Enable_D

Technology Intent | Scripting

- [x] Default
- [ ] Nominal only
- [ ] Nominal & Monte Carlo
- [ ] My Script 1
- [ ] My Script 2
- [ ] My Script 3

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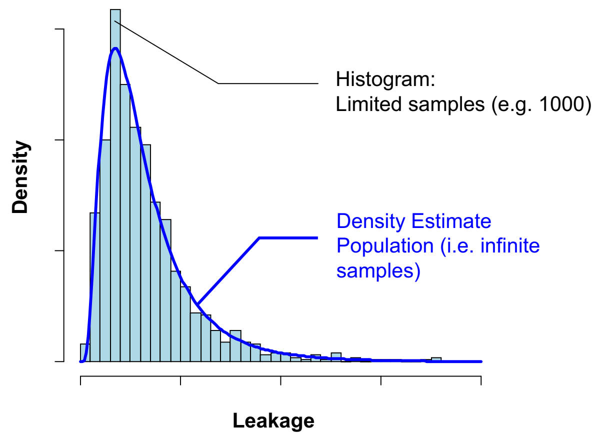
Results—Histogram & Density Estimate

Example results for 65nm library



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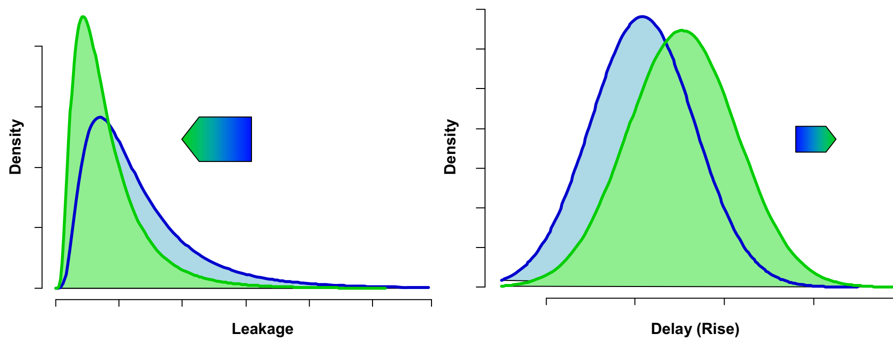
Results—NAND-Gate

Example results for 65nm library



Leakage
- Median leakage reduced by 37%
- Standard deviation reduced by 35%

Delay
- Median delay increased by 5%
- Small increase in active area

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Results—Summary

Example results for 65nm library

Cell	Transistors	Design Parameters	Yield Improvement
invd2	4	6	**+ 9%**
buffd4	12	10	**+ 10%**
nd2d2	8	11	**+ 13%**
mux2d2	14	26	**+ 11%**

- Average yield improvement of 11%
  - *Yield: Percentage of circuits meeting given specification*
- Variability reduction of 25%-35%
- Tradeoff
  - *Area increase 10%*
  - *Delay increase max. 5% (constraint for optimization)*

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Conclusion

- Considering process variations becomes increasingly important for digital cells
- Time pressure for library qualification requires automated optimization
- Optimization tool a must for tradeoff analysis
- Synopsys/MunEDA library migration flow successfully addresses process variations
- Promising results from first library migration (65 nm)

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Backup Slides

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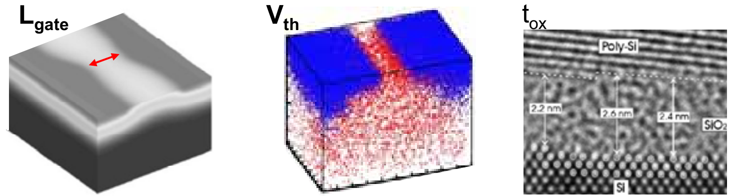

Local Process Variations

L_{gate} V_{th} t_{ox}

- Source:
  - *Line edge roughness*
  - *finite number of dopant atoms*
  - *gate oxide variation*
- Local variations cause a production-induced asymmetry of symmetrically designed devices ➔ Mismatch

Figures from IBM

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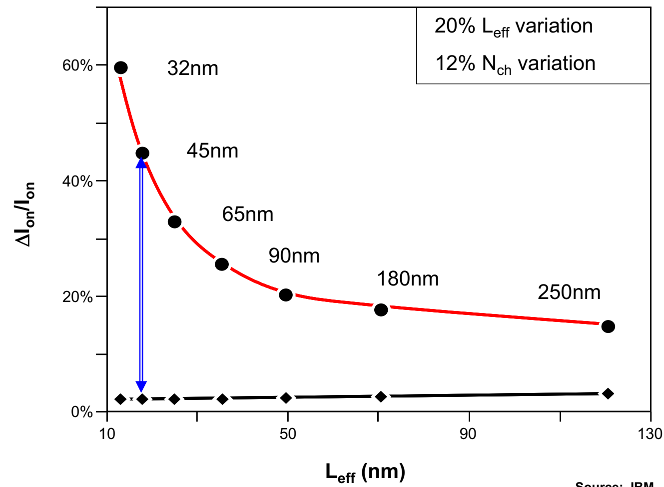
Trend of Local Variations on Digital Cells



Source: IBM

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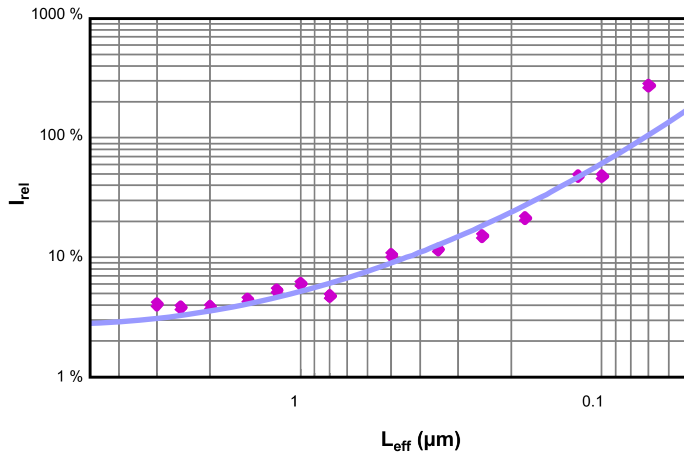
Trend of Local Variations on Analog Cells



Data: K. Bult (ESSCIRC 2000)

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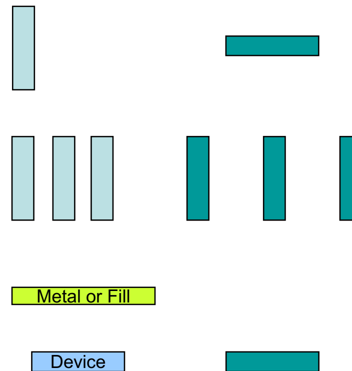
Variation Components (Proximity)

- Properties depend on orientation, proximity to other features, and presence of covering metal or fill pattern
- Important for analog and high performance digital including cell based designs
- *Deterministic systematic variation that can be modeled and/or mask compensated*



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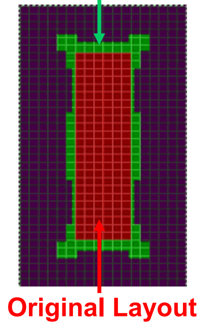
Optical Proximity Correction (OPC)

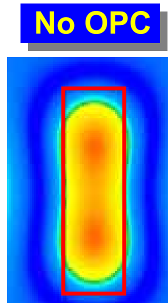
- Corrective modifications to improve process control
  - *improve yield (process window)*
  - *improve device performance*

OPC Corrections

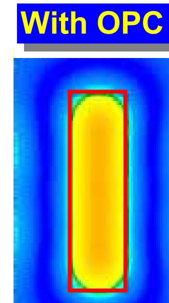


Original Layout

No OPC



With OPC



Source: Synopsys

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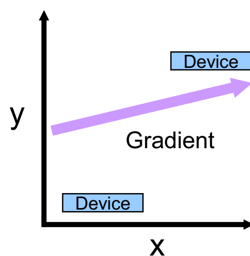
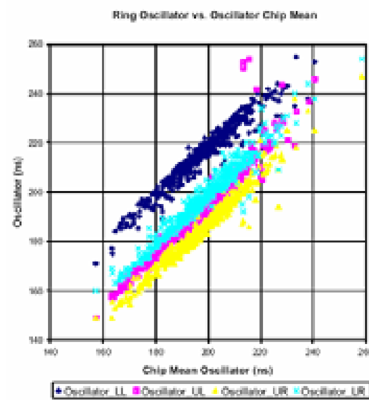
Variation Components (Spatial)

- Process, thermal, and stress gradients lead to position dependent variation
- Important for analog (DAC, ADC, PLL, CDR) and clock skew on large digital chips
- Typical value in literature is 1%/mm





7.5% within chip variation

Zuchowski et al (IBM) ICCAD 2004

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Design Elements and Variability

		Global	Local
Analog	Single ended	●	Large devices
	Differential	Designed out	●
Standard Cells		●	●
Memory Cell & Sense Amps		●	●

Source: Synopsys

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