Design For Yield (DFY) Concepts for Analogue and Mixed-Signal Circuits

Michael Pronath – MunEDA GmbH

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Overview

- Circuit DfY in the design flow
- Application examples
- Worst-case Analysis and Diagnosis
- Comparison to digital corners and Monte Carlo
- Operating conditions and Yield
- Mismatch in analog circuits
- Summary: What‘s special about analog DfY ?

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Field of Application

- Application: Full-custom circuit design at the transistor level
  - Analog & Mixed signal (A/MS) cells like operational amplifier, filter, PLL
  - Digital library optimization, full custom logic
  - Memory
- Where in the design flow?
  - Sizing of transistor geometries (after topology selection, before layout)
  - Analysis and compensation of parasitic influences in extracted view (after layout)
- Goals
  - Performance
  - Robustness against parametric process variation and operating conditions

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WiCkeD Applied to Customer Circuits and Technologies

Circuits:

- Adiabatic Logic Gates
- Bandgaps
- Buffer chains
- Bypass Filters
- Cascode Gain Stages
- CCOs
- Charge Pumps
- CML Converters
- Comparators
- Constant Voltage Sources
- Current Mirrors
- Current Sources
- Current Mirror OpAmps
- Differential Amplifiers
- Filters
- Folded-Cascode OpAmps
- Fully Differential OpAmps
- High Voltage Circuits
- Latches
- Level Shifters
- Low Voltage Circuits
- Operational Amplifiers
- PLLs
- Receivers
- RF-Circuits
- Ring Oszillators
- Sense Amplifiers
- Sensor Circuits
- Single-Stage Amplifiers
- Transceivers
- VCOs

Technologies:

- From 1µ down to 90n CMOS
- Projects in 65n CMOS started
- BiCMOS, BCD, Bipolar…

Applications:

- Memory
- Wireless Communications
- Wirebound Communications
- Automotive & Industrial
- Sensors
- Consumer & Standard ICs…

More than 250 design projects since 2002

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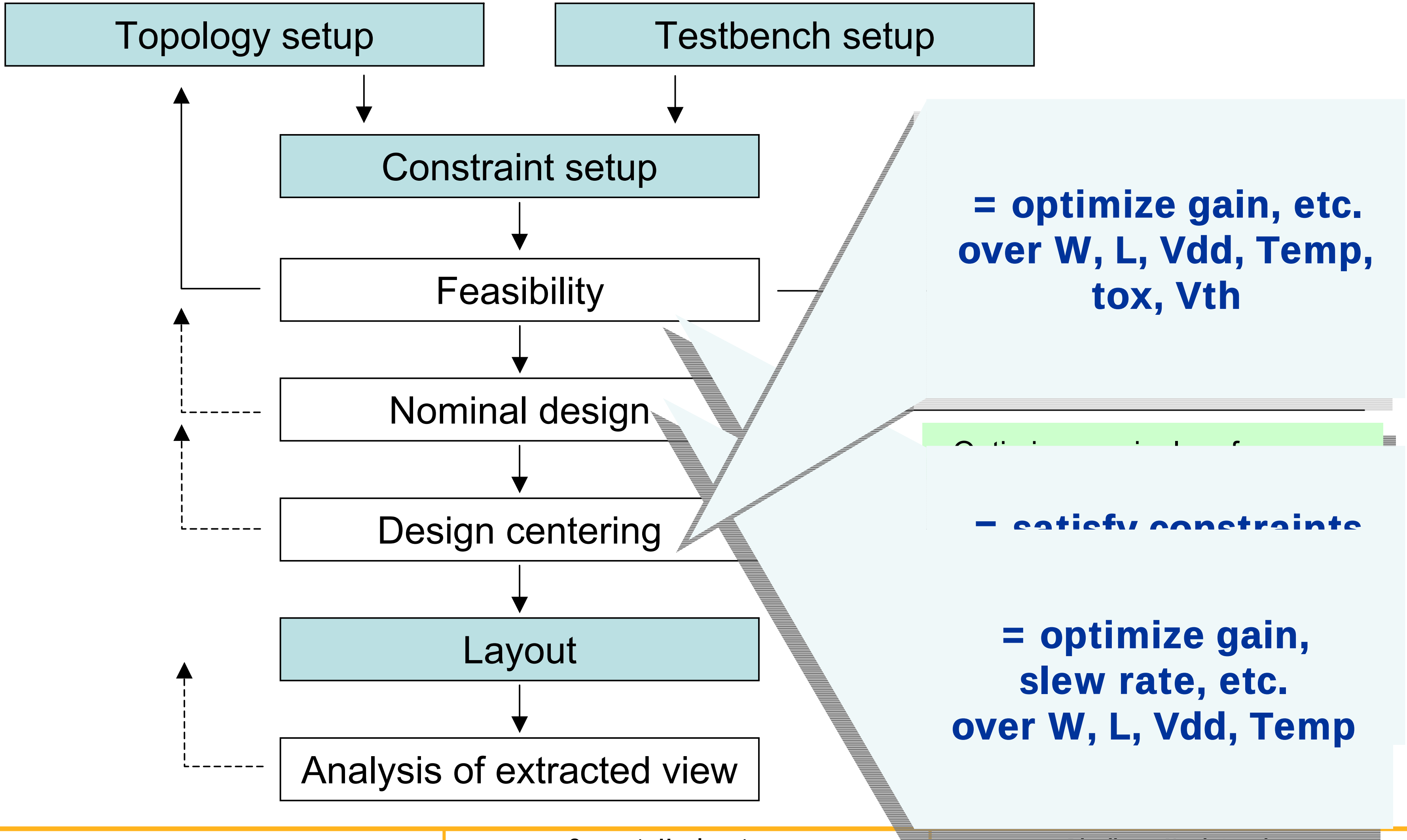
Workflow with WiCkeD



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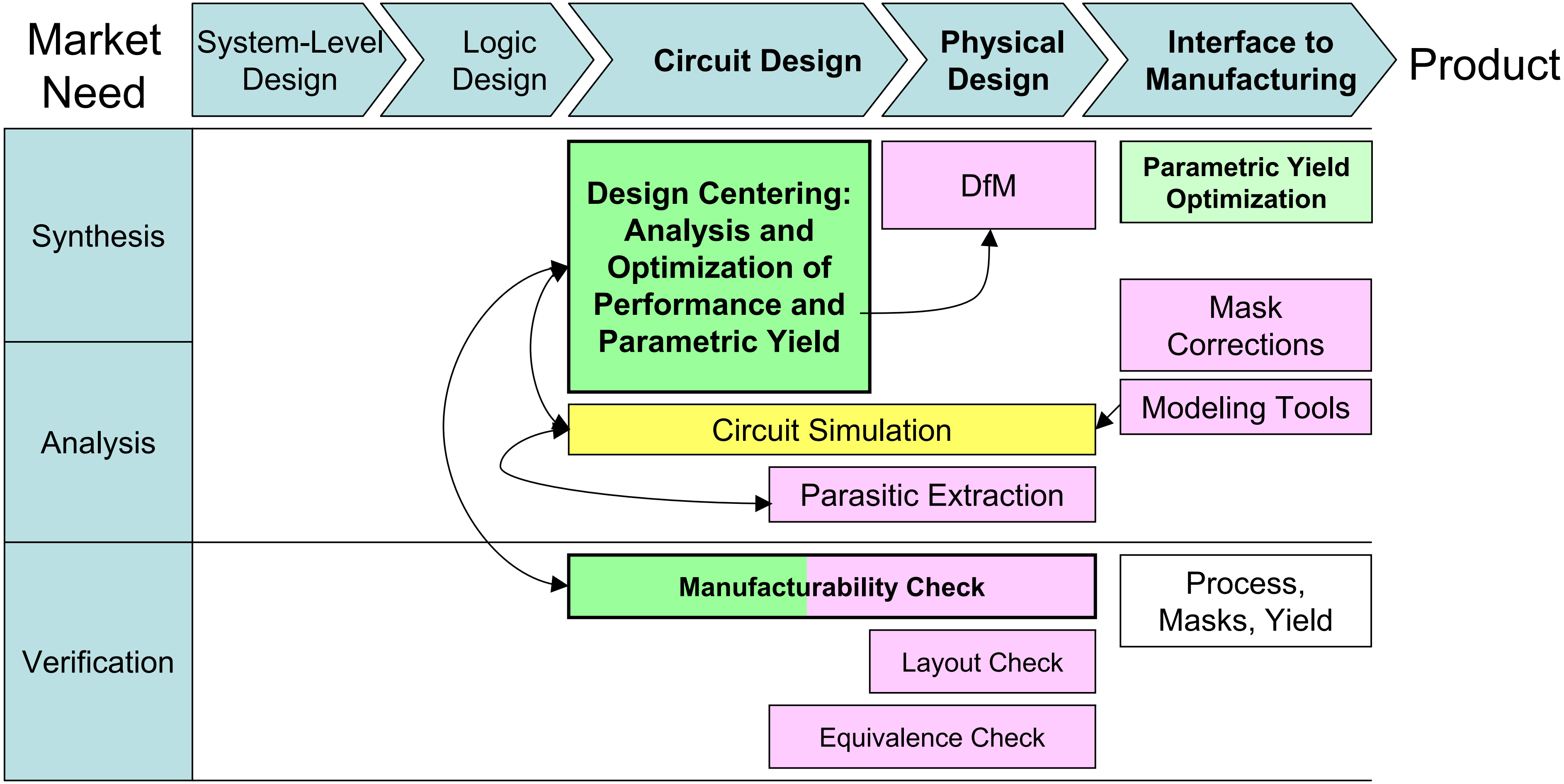
DFM / DFY - Design Centering and Yield Optimization in the AMS / RF Flow



Source: SIA ITRS 2003

Circuit Simulation | **Layout, DFM, Physical Design** | **Design Centering / Yield Optimization**

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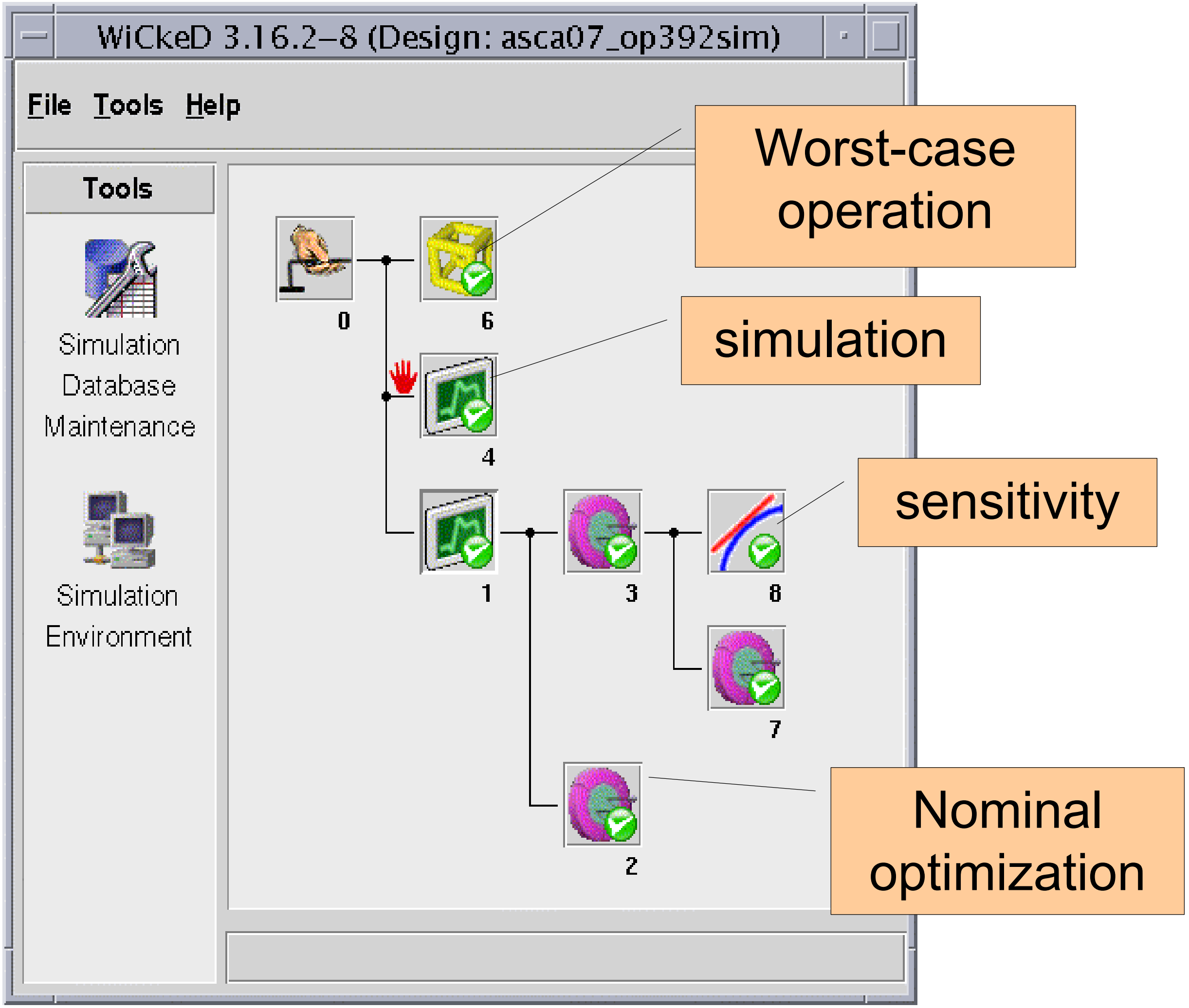
WiCkeD Main window (example)

The history tree grows from top left to bottom right



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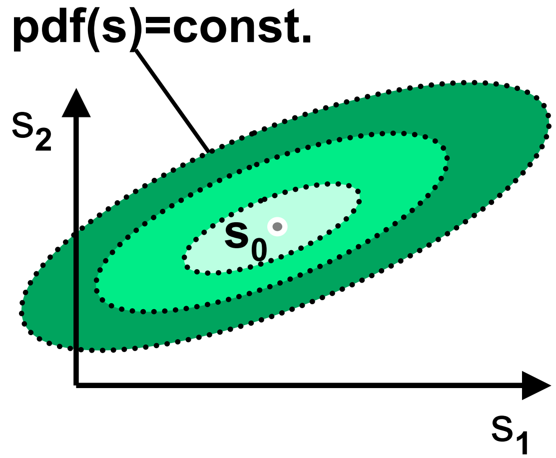
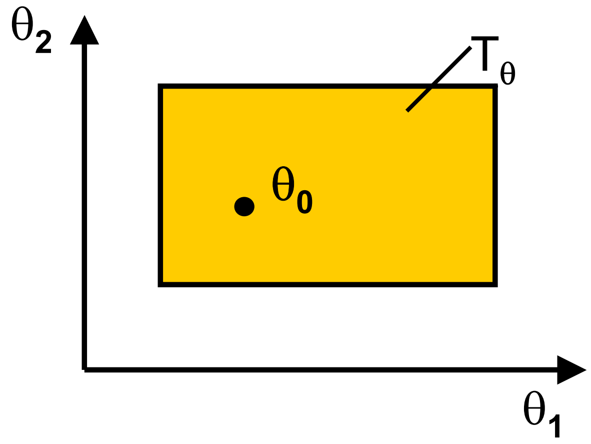
Three parameter spaces

- **Design parameters** **d**
  - *for instance widths and lengths of transistors*
  - *are adjustable by the designer*



- **Process parameters** **s**
  - *for instance tox, vth*
  - *global and local (mismatch)*
  - *random variation*

- **Operating parameters** **θ**
  - *for instance vdd, temperature*
  - *range of operating conditions*



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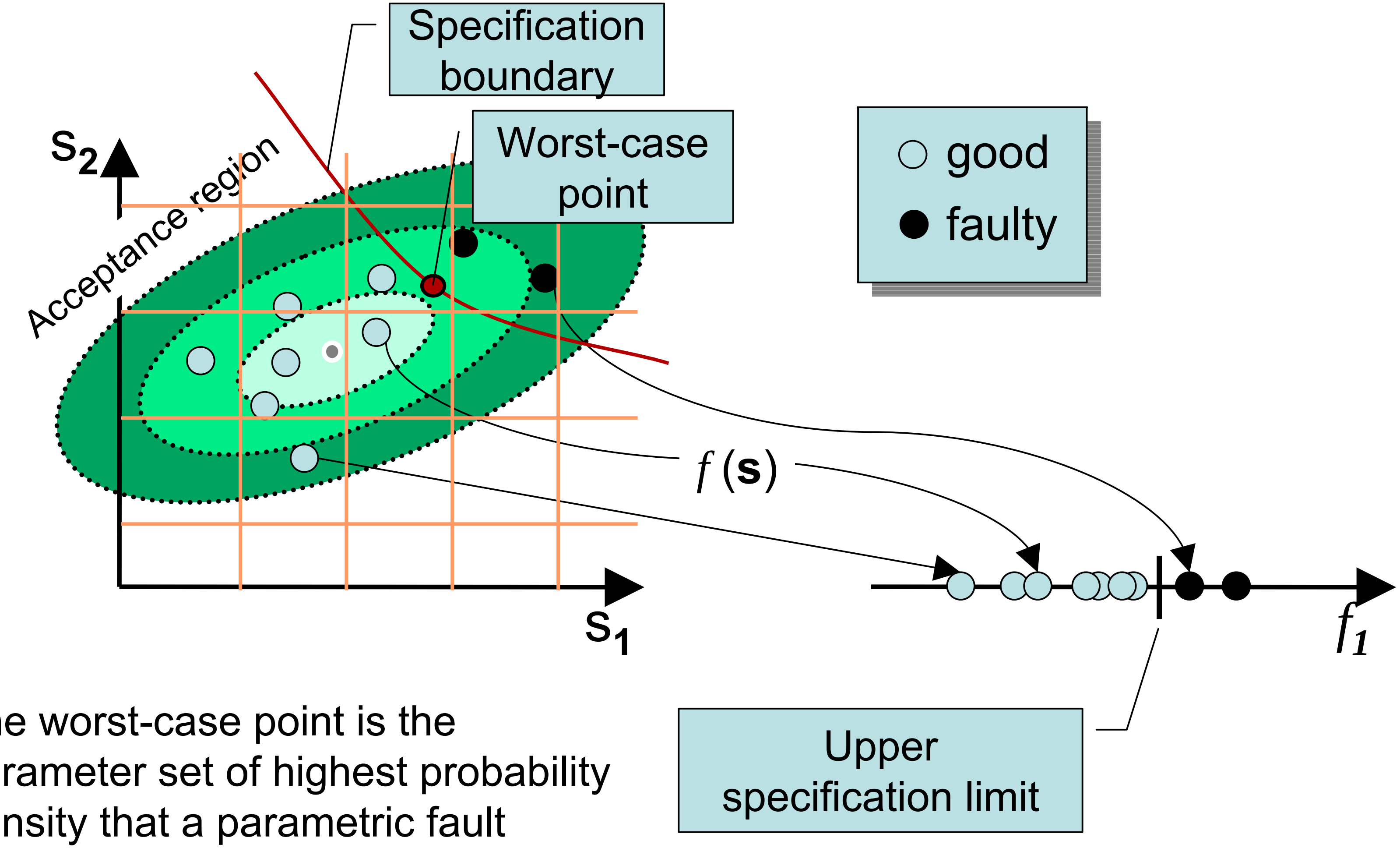
Worst-case point



The worst-case point is the parameter set of highest probability density that a parametric fault occurs.

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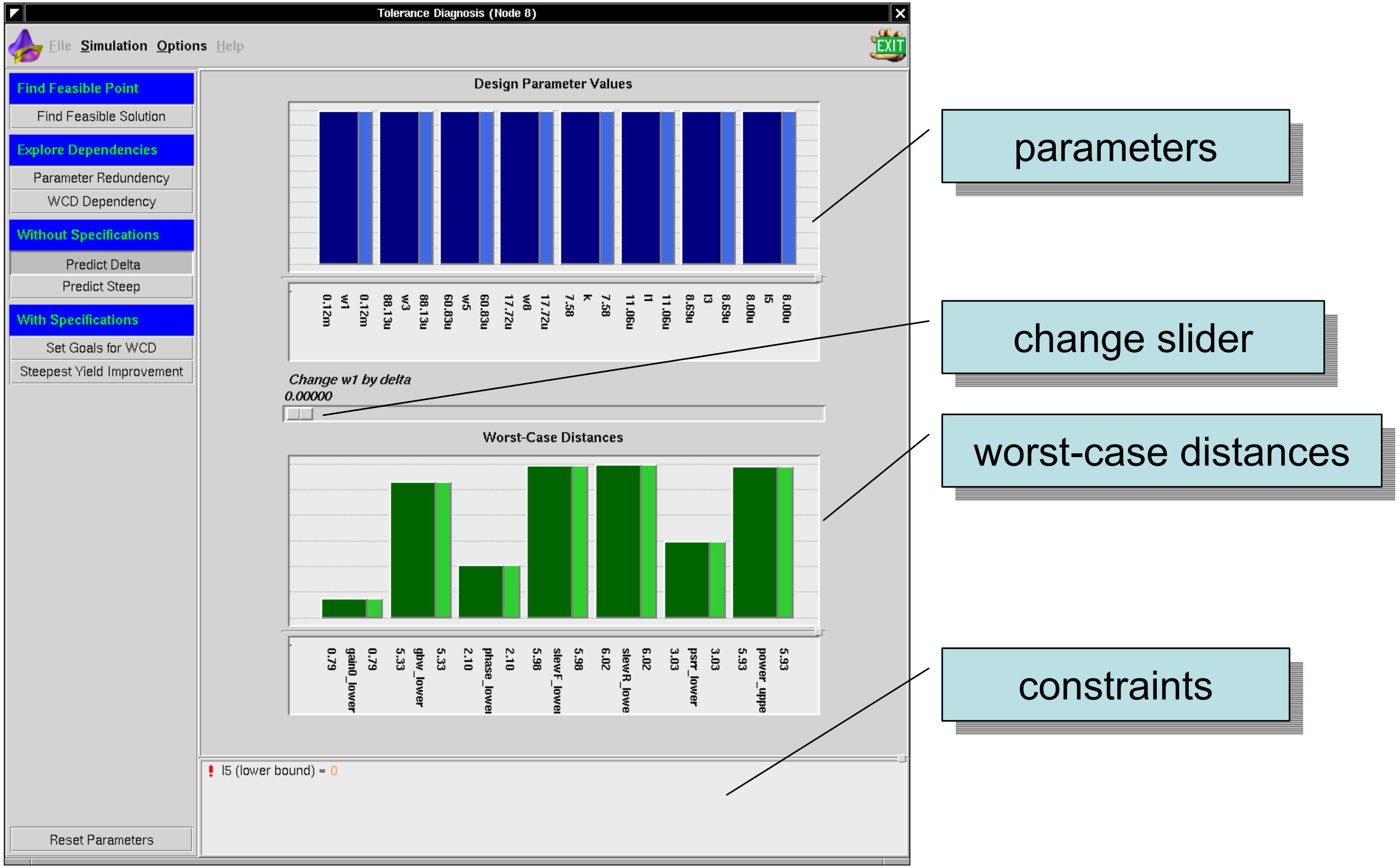
Worst-case Diagnosis



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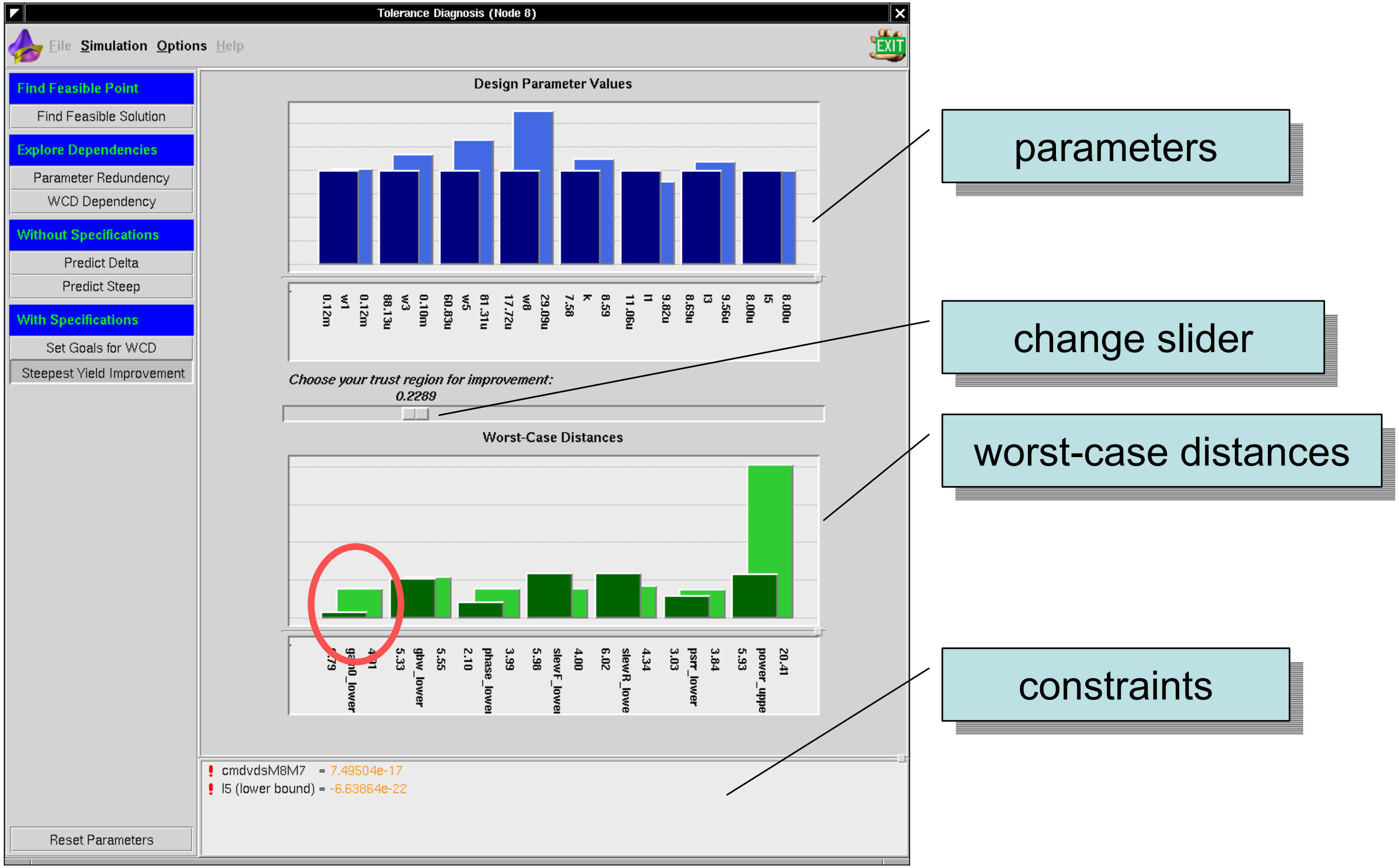
Worst-case Diagnosis



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Worst-case points vs. digital corners vs. Monte Carlo

	WCD	S/F Corner	Monte Carlo
reflects technology	✓	✓	✓
topology dependent	✓	⛔	✓
analog performances	✓	⛔	✓
yield estimation	✓	⛔	✓
mismatch	✓	⛔	✓
yield improvement	✓	⛔	⛔
efficiency	+	++	– –

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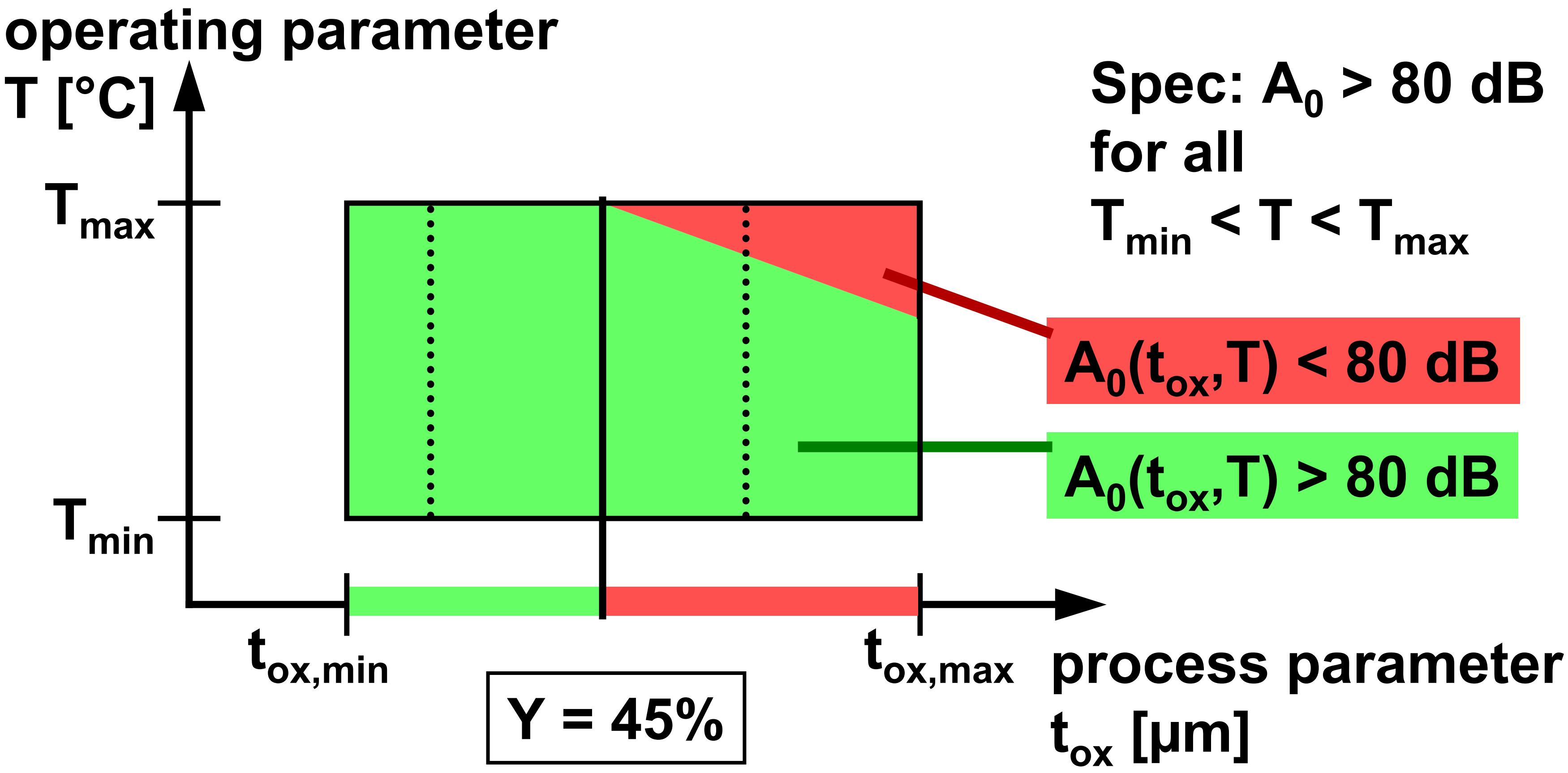
Monte Carlo-Analysis incl. Operating Conditions



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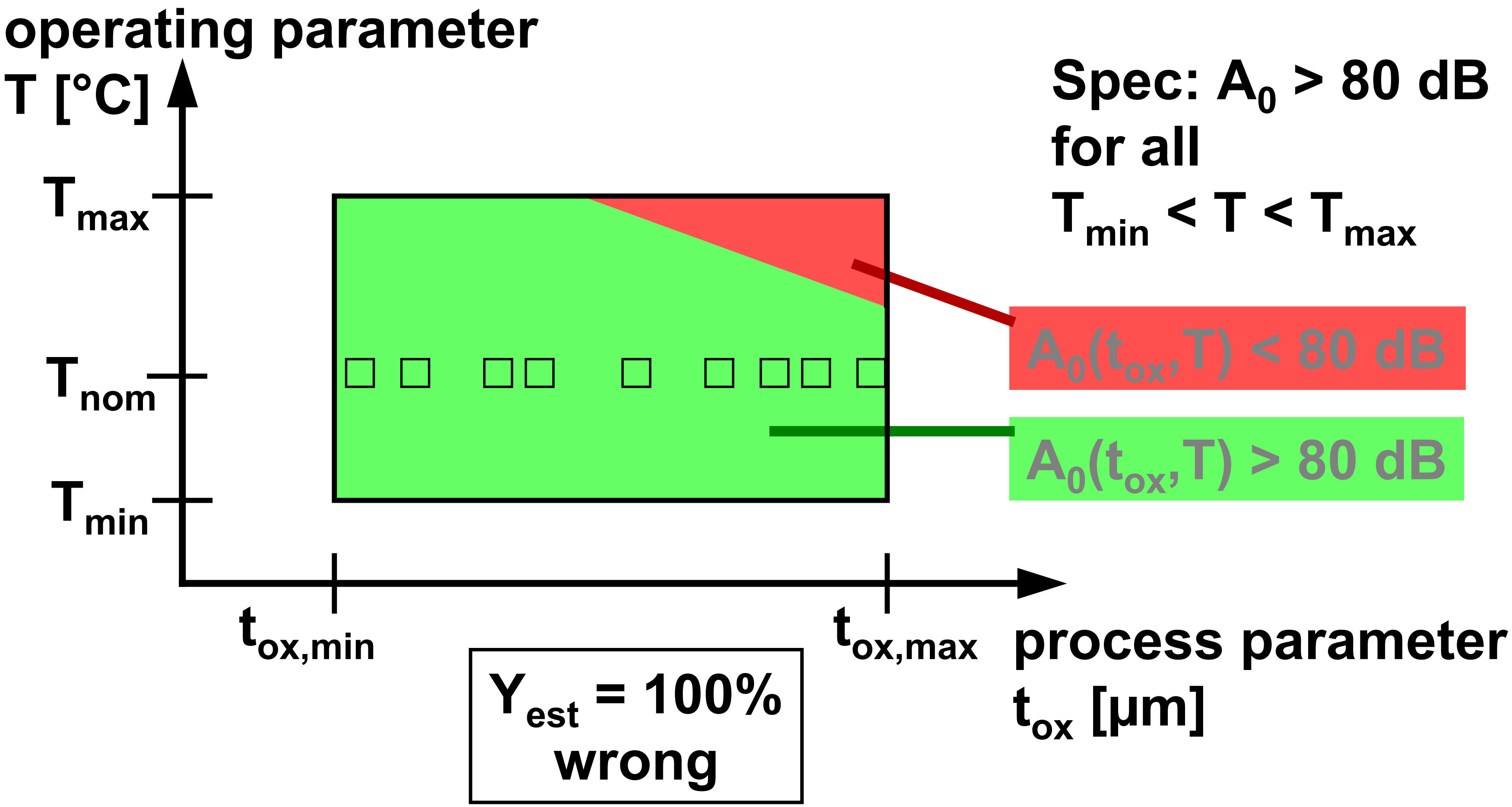

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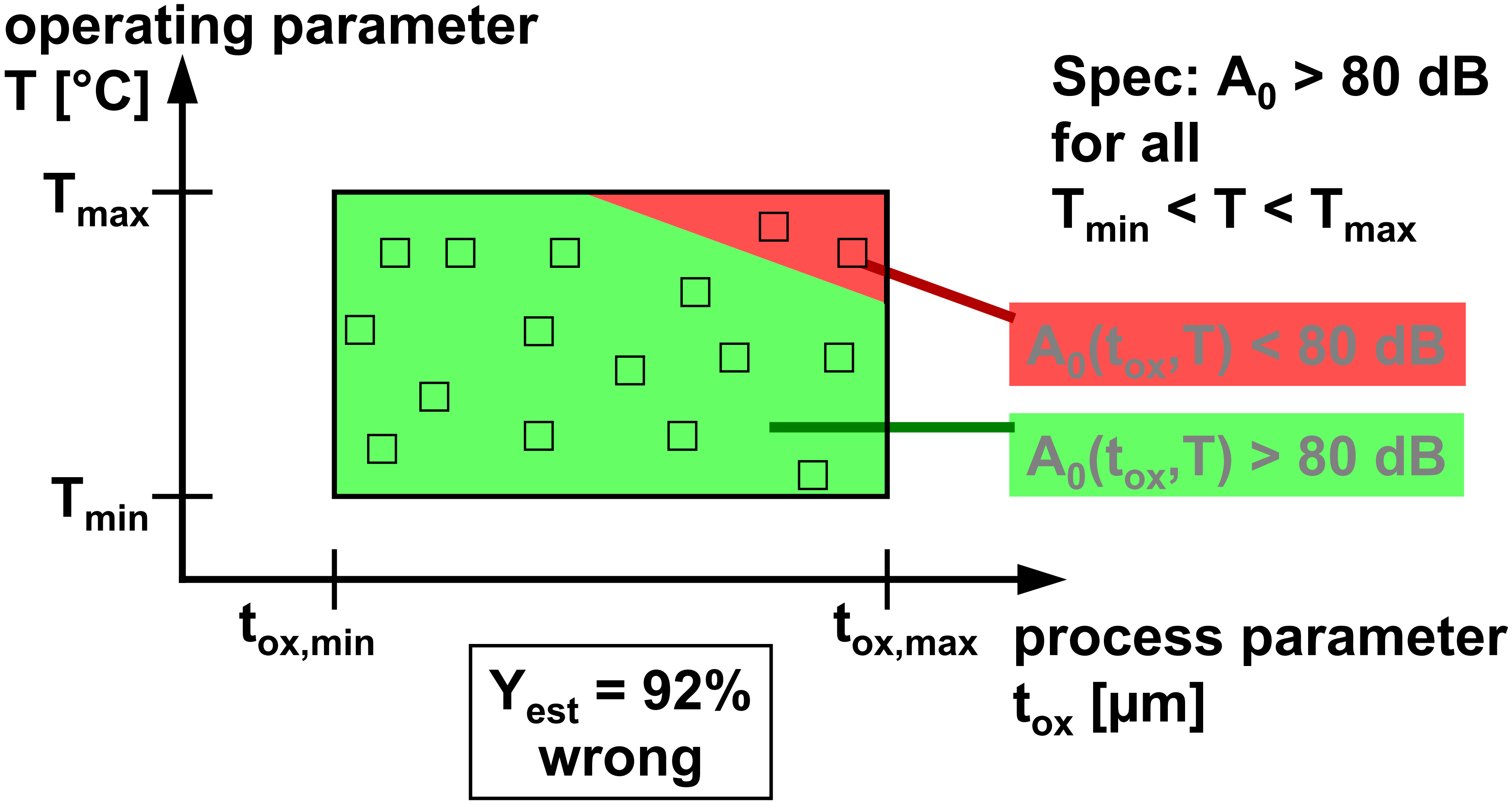

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Monte Carlo-Analysis incl. Operating Conditions

- Sweep over operating condition for each sample element
  - very high effort
  - For multiple operating parameters (VDD, T, I_{bias}, C_{load}, ...) the effort increases exponentially
- Simulation at the worst-case operating conditions
  - is specific for each specification
- Both approaches can be combined

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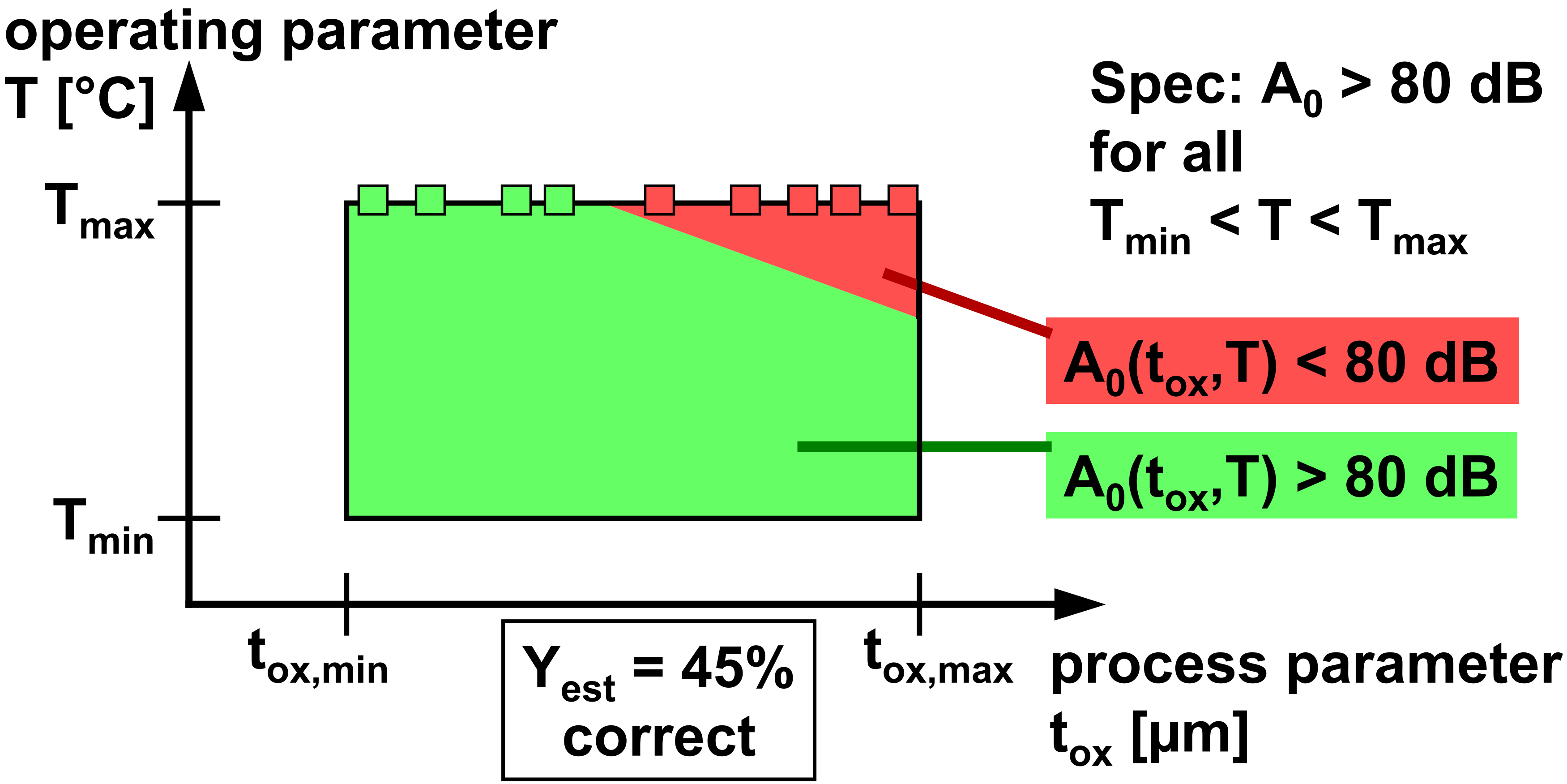
Monte Carlo-Analysis incl. Operating Conditions



Monte Carlo-Analysis of A_0 over t_{ox} at $T = T_{max}$

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Monte Carlo-Analysis incl. operating conditions

Samples in (t_{ox},v_{th})

↓

Example:

Simulation of

A_0 (t_{ox},v_{th})	for T_{max},VDD_{min}
Ft (t_{ox},v_{th})	for T_{min},VDD_{min}
Power (t_{ox},v_{th})	for T_{max},VDD_{max}

↓

distributions, moments, ...

Partial yields Y_{A0}, Y_{Ft}, Y_{Power}

Total yield Y

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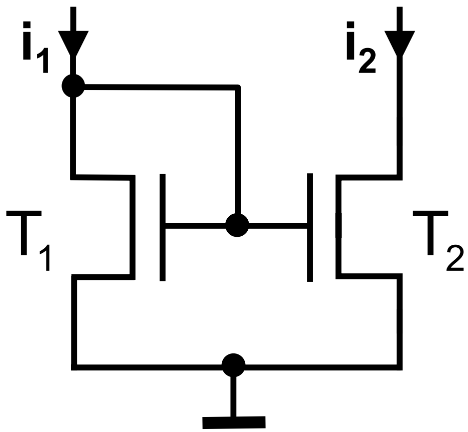
Mismatch

- **Analog circuits are based on symmetries**
- **Mismatch = asymmetry caused by local variation**

Example: Current mirror



$$i_2 = k\left(\sqrt{\frac{i_1}{k}} + \underbrace{Vth_1 - Vth_2}_{\Delta Vth}\right)^2$$

Mismatch: $\Delta Vth \neq 0 \quad \Leftrightarrow i_2 \neq i_1$

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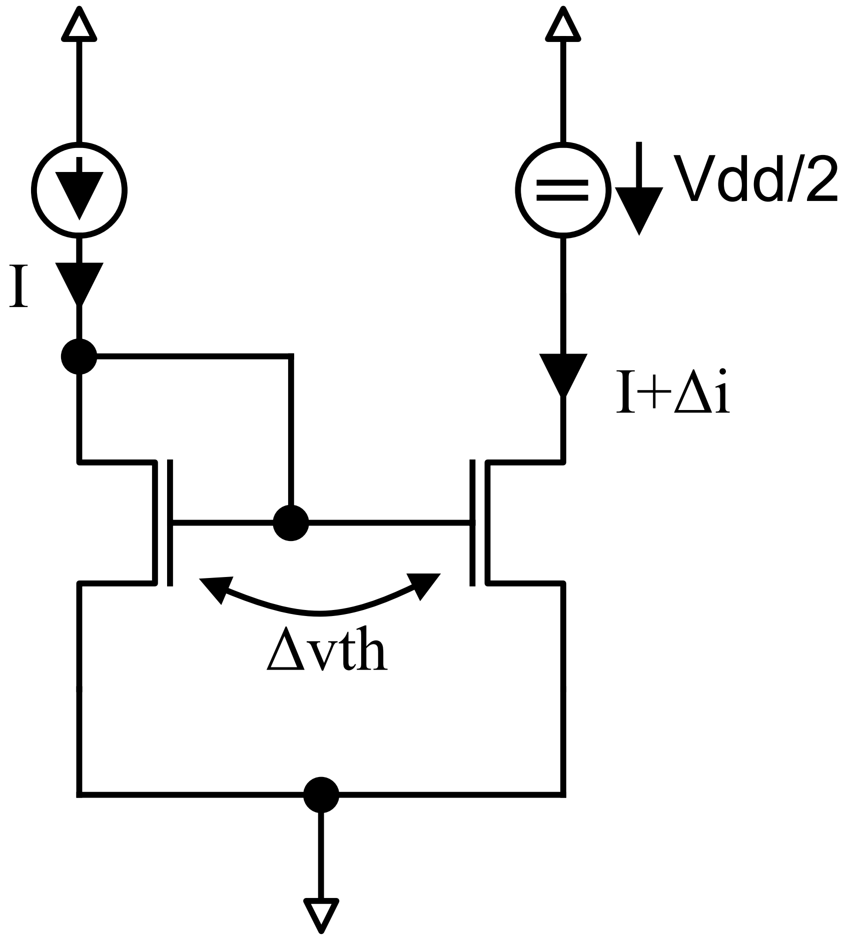
Current Mirror: „small signal“ mismatch



$$\Delta i = g_m \cdot \Delta vth$$

$$\sigma_{\Delta i} = g_m \cdot \sigma_{\Delta vth}$$

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Mismatch Influence

$$\sigma_{\Delta i} = g_m \cdot \sigma_{\Delta vth}$$

Biasing:

$$I = k\frac{W}{L}(V_{gs} - V_{th})^2$$

$$g_m = \frac{\partial I}{\partial V_{gs}} = 2k\frac{W}{L}(V_{gs} - V_{th})$$

$$= 2\sqrt{k}\sqrt{\frac{W}{L}I}$$

Pelgrom's Area Law:

$$\sigma_{\Delta vth} = \frac{A_{mm}}{\sqrt{W \cdot L}}$$

$$\sigma_{\Delta i} \propto \sqrt{\frac{W}{L}} \cdot \sqrt{I} \cdot \frac{1}{\sqrt{W \cdot L}} = \frac{\sqrt{I}}{L}$$

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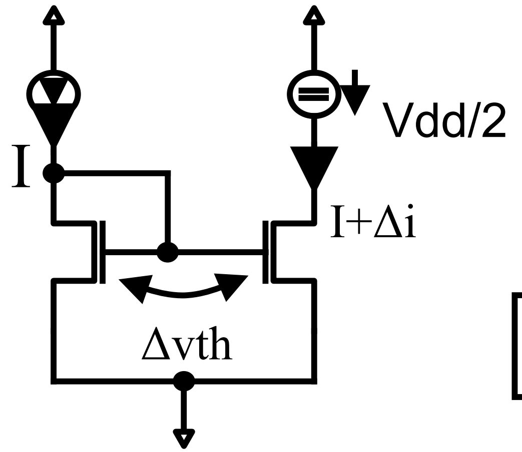
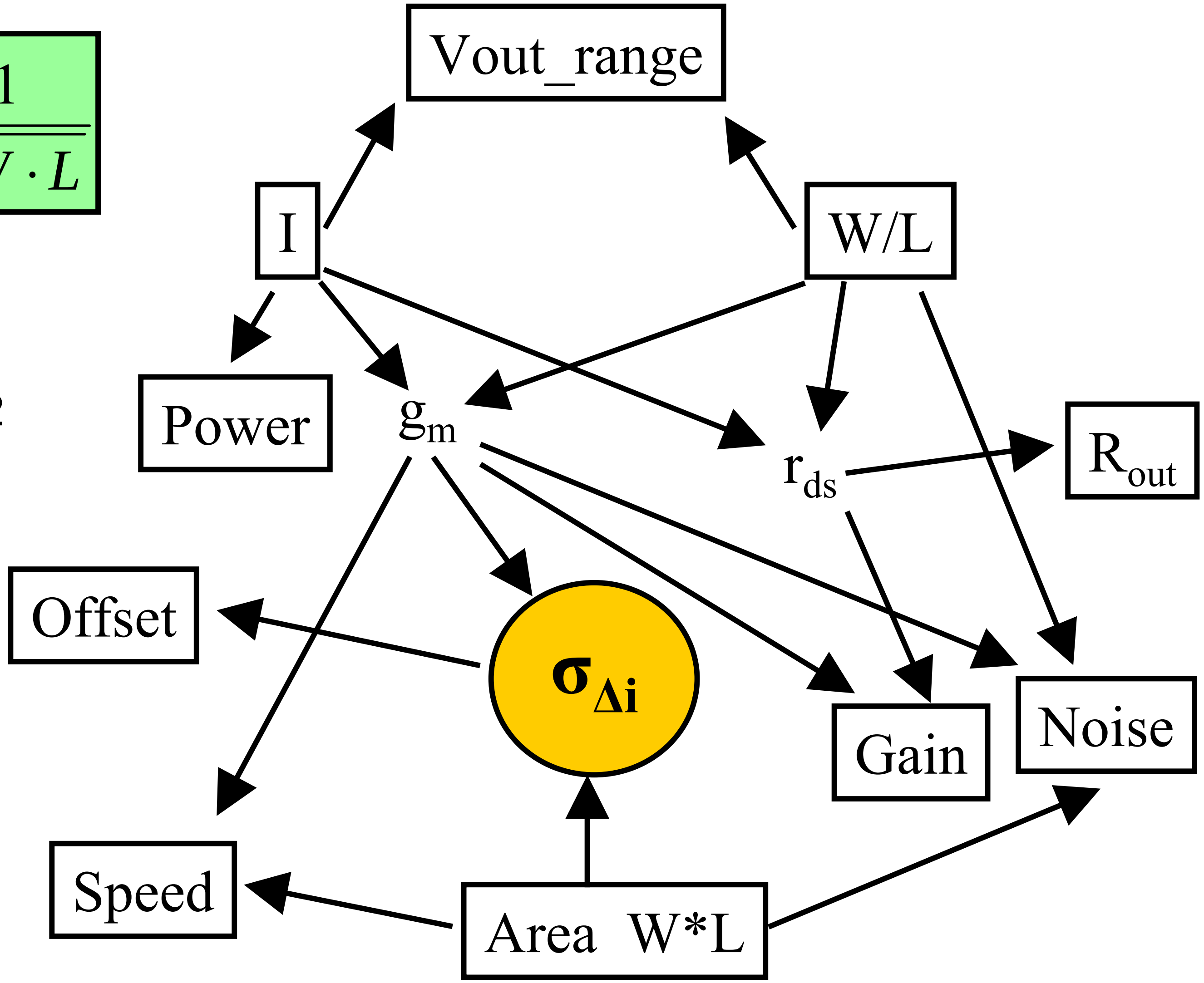
Mismatch Tradeoffs

$$\sigma_{\Delta i} \propto \sqrt{\frac{W}{L}} \cdot \sqrt{I} \cdot \frac{1}{\sqrt{W \cdot L}}$$





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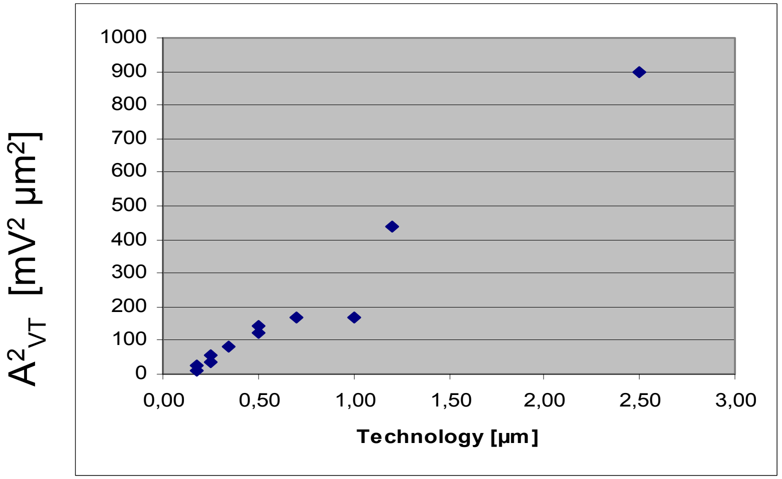
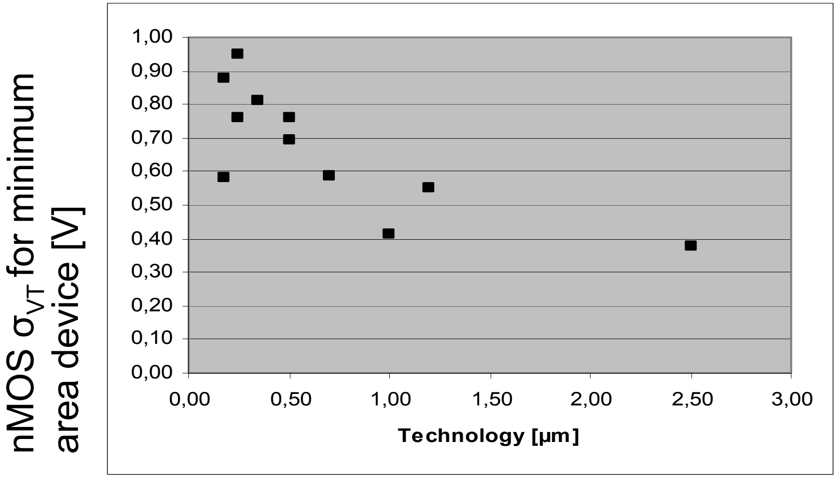
Mismatch (3)

- Variance of V_{th} depends on device area: $\sigma^2_{VT} = A^2_{VT} / (W \cdot L)$
- Problem grows with scaling:
  - A^2_{VT} decreases only linearly with the minimum feature size, therefore the variance of the minimum area device grows
  - Decreasing Vdd increases relative error $\sigma_{VT} / V_{in\ RMS}$
- Analog circuits cannot be simply scaled.





Source: Peter R. Kinget (IEEE Journal of Solid-State Circuits, 06/2005)

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What‘s special about Analog DfY ?

- Yield of complex performances
  ⇒ Clear separation of design, process, and operating conditions
  ⇒ Individual worst-case points instead of pre-defined corners
- Designer‘s expert knowledge is important
  ⇒ Allow strong user interaction and a design strategy
  ⇒ Focus on analysis and incremental interactive design steps, instead of black-box „synthesis“
- Many constraints per transistor
  ⇒ saturation, current symmetries, etc.
  ⇒ Efficient algorithms for typical analog problem sizes

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