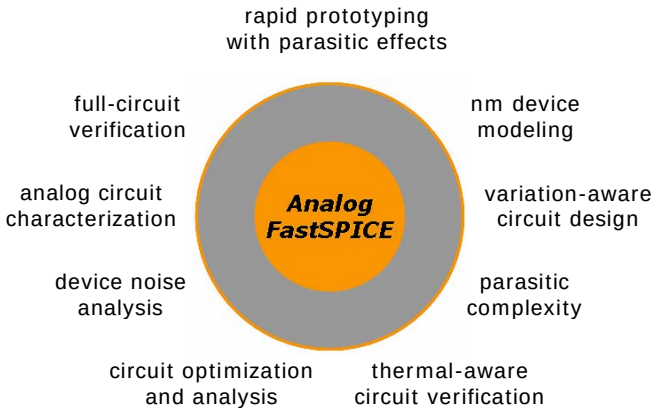
The nanometer Circuit Verification Forum

Hosted by Berkeley Design Automation

TechMart Santa Clara, CA

September 22, 2011

Program Announcement



The *nanometer Circuit Verification Forum* will be held in Silicon Valley, CA the day after the 2011 Custom Integrated Circuits Conference (CICC).

Hosted by Berkeley Design Automation, in collaboration with selected EDA, industry, and academic partners, the forum will showcase advanced nm circuit verification technology and techniques.

This gathering of leading-edge technologists will provide an outstanding opportunity to share experiences and best practices, and to network with nm circuit designers.

Analog, mixed-signal, RF and custom digital circuitry is the biggest differentiator and the most difficult design and verification challenge for nm ICs. Implemented in GHz nm CMOS, these circuits introduce a new class of verification challenges that traditional methodologies cannot adequately address.

The *nm Circuit Verification Forum* is a technical event that will address these challenges in detail. Speakers will present and demonstrate proven, industrially-relevant solutions as applied to production nm circuits from ADCs and PLLs to RFICs and high-speed I/O. This is the ideal forum for hands-on circuit designers wishing to learn more about pressing nanometer issues and design managers desiring to improve the comprehensive verification performance of their teams.

Agenda

9:00	Registration
9:30	Welcome and Keynote
10:00	Morning sessions (including break)
12:30	Lunch
1:30	Afternoon sessions (including break)
4:30	Solution demonstrations and reception
6:30	Forum wrap-up and close

Application Examples

- Data converters
- PLLs and timing circuits
- High-Speed I/O
- Image sensors

Emerging verification technologies

- Nanometer device modeling
- Rapid prototyping including parasitic effects
- Thermal-aware circuit verification
- Variation-aware circuit design
- Circuit optimization and analysis

To register visit: www.nm-forum.com

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