

Circuit Sizing & Design Centering with MunEDA WiCkeD in TSMC RF Reference Design Kit 2.0 (RF RDK 2.0)

AMS/RF circuit design becomes challenging in sub-100nm technologies for many reasons like lower core voltages, less headroom, more on-chip variation and other effects that can affect performance, robustness and yield of critical circuit designs.

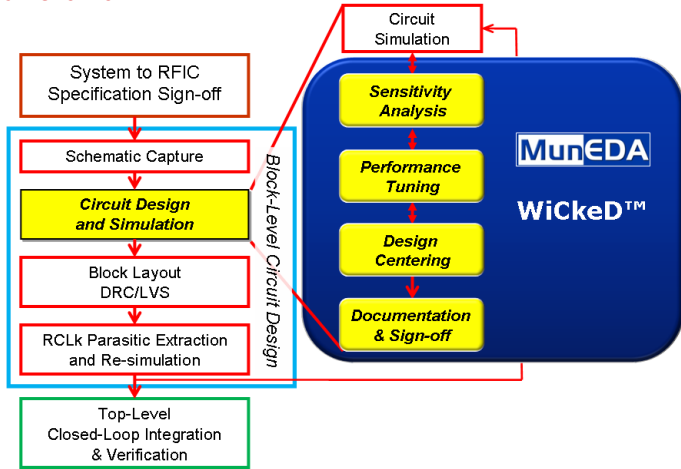
Design Challenges Today

- **Circuit Design got more difficult in sub-100nm technologies**
 - Lower core voltages, less headroom, more leakage
 - Growing impact of local variation, other new effects
- **Process scaling of AMS/RF designs is expensive**
 - With every new process node many existing designs are to be ported to the new target process
 - Analog scaling is not as straight-forward as digital
 - gets more difficult with sub-100nm processes
 - can be the bottleneck for SoC design re-use

New solution introduction

- **MunEDA WiCkeD™**
 - Specification-driven environment for interactive & automatic performance analysis, and sizing
 - Circuit-independent, process-independent
 - Fast, simulation-based, flexible design strategy, customer- and silicon-proven
- **Typical application fields**
 - Demanding AMS/RF designs, high speed digital I/O, memory, automotive, communication, consumer electronics
 - Tuning trade-offs of noise / power / area / speed / ... considering process variation & mismatch
 - Design centering within the process window to reduce the risk of redesigns and parametric yield problems

Flow Overview



WiCkeD - Software Features

- Sensitivity analysis (Design Parameters, Process, Mismatch, Operating conditions)
- Worst-case analysis (Process, Mismatch, Operating conditions)
- Monte Carlo analysis
- Feasibility optimization (structural constraints, operating point)
- Nominal sizing (manual, automatic: deterministic / global)
- Design centering (parametric yield optimization)
- Interactive Design History
- Parallel distributed simulation interface supports industry standard simulators

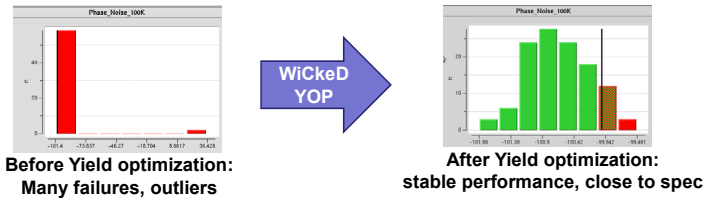
"We are proud that TSMC has selected MunEDA WiCkeD to be integral part of the TSMC RF RDK 2.0", stated Michael Pronath, MunEDA Vice President Products & Solutions. "Our cooperation with TSMC and our mutual customers showed that specification driven design and statistical design are important for successful high-end circuit design in modern process technologies."

Circuit designers use MunEDA's tool suite WiCkeD to balance specs, area, power, reliability and robustness. WiCkeD can automate manual circuit design tasks in IP porting and cell migration to maximize designers' efficiency.

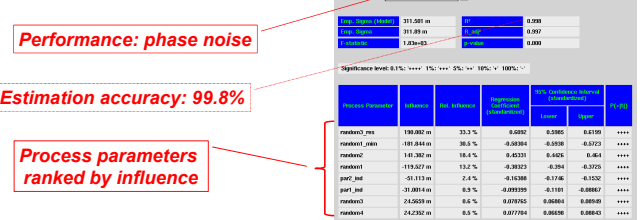
Test Case Introduction – VCO Voltage Controlled Oscillator Performance & Yield Optimization in 2 Steps

- **Test Case description**
 - VCO, 65nm, 2.475GHz
- **Test Case validate feature**
 - Automatic Performance Tuning
 - Automatic Yield Optimization
 - Sensitivity to process variation and mismatch
- **Before**
 - kVCO=40MHz/V
 - Phase noise -99dBc/Hz @ 100k, -123dBc/Hz @ 1M
- **Step 1: Performance Improvement**
 - kVCO=70MHz/V
 - Phase noise -101dBc/Hz @ 100k, -126dBc/Hz @ 1M
- **Step 2: Yield Improvement by 50%**

VCO Tutorial – Yield Analysis by WiCkeD Monte Carlo



WiCkeD Sensitivity Analysis



With/Without new solution comparison

Topic	Conventional Design Style	Using MunEDA WiCkeD™
Specification-driven circuit design	– Uncontrolled overdesign spending area and power for random safety margins on all specs	+ Balance specs, area, power and process robustness VCO: phase noise reduced by 3dB
Circuit design re-use for new spec	– Migrate a large number of cells in pure manual labour	+ Automate sizing tasks to maximize designers' efficiency VCO: designer efficiency +50%
Circuit design for yield	– Limited analysis capabilities, guesswork, trial-and-error	+ Fast design centering in a controlled environment VCO: fully automatic yield improvement +50%

Summary - Benefits of using MunEDA WiCkeD™

- Improve robustness of designs against parametric process variation
 - to reduce risk of redesigns
 - easier ramp-up to high volume parametric yield
- Achieve difficult performance goals, power and area requirements
- Optimal use of the process technology's capabilities
- Improve designers' efficiency to reduce design time

"MunEDA complements our RF RDK 2.0" stated Tom Quan, Deputy Director of Design Methodology & Service Marketing at TSMC. "We are happy to collaborate with MunEDA, the experts on statistical circuit analysis and specification-driven circuit design automation. WiCkeD delivers a substantial benefit to the designers using TSMC technology and was validated for TSMC's 65nm RF RDK 2.0."