



Phase 1 extends from July 2007 to December 2008

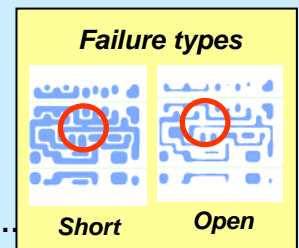
The partners mainly focus on developing **tools and models** until **prototype level**, and proposing **first test structures**

Prototypes (examples)

- A generator of circuit topologies using a hierarchical block-based algorithm
- TechModeler modeling software
- 45 nm CMP model calibration structures

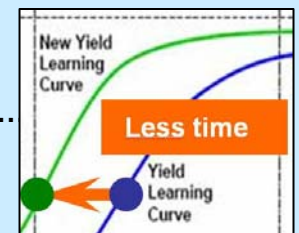
Some illustrative 65 nm test chips

- Monitor for Negative Bias Temperature Instability
- Monitor for failure localization
- Efficiency of the anti-fuse solution proven on silicon



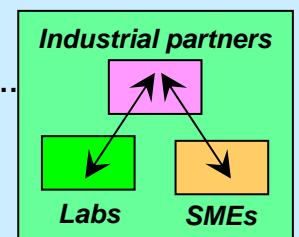
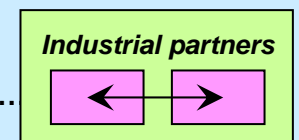
First metrics

- **Yield learning curve:** Thanks to the yield test-chip, the learning speed for 45 nm has been accelerated of about 20-30%
- **Performance:** Optimized bipolar transistors increased Voltage Amplifier bandwidth from 110 to 150 MHz
- **Consumption:** In-field programming architecture: power consumption during programming is reduced by 5X in 45nm vs 65 nm



Examples of cooperations

- Horizontal cooperations
- ▶ On library yield, by comparing results from *Yield & Reliability optimised Libraries* (Infineon) and *Circuit & Library Yield System* (ST-F)
- ▶ Complementarity of *Post-layout processing* (ST-F) and *Place & Route* (Infineon) for an upgraded yield-oriented back-end flow
- ▶ Know-how exchange on *modeling* (Infineon) and *monitoring* (ST-F)
- Vertical cooperations
- ▶ ST with Dolphin/InfiniScale/IMEP/MunEDA/Xyalis
- ▶ Infineon with InfiniScale/MunEDA...



Public events – Workshops

- Session on *Design for Yield / Reliability* at MEDEA+ DAC, Leuven, May 27, 2008
- Common HONEY-ROBIN Workshop on DFM, Paris, June 24, 2008