Analysis and optimization of a CMOS mixer circuit with WiCkeD

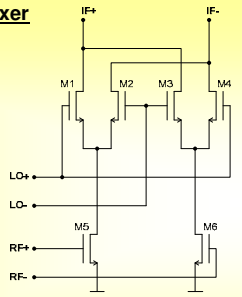
Challenges of Mixer Optimization

There are very special challenges for the optimization of a mixer circuit. One is that special RF analyses are required, e.g. Periodic Steady State analysis (PSS) and Periodic Small Signal analyses. Another one is the application of OCEAN post processing functions to calculate mixer performances, like noise figure or intercept points

Introduction to Gilbert Cell Mixer

Circuit Description:

- Double-balanced mixer (Gilbert Cell)
- Gilbert Cell mainly consists of 3 differential pairs
- Small RF signal is applied to M5,M6
- Large LO signal is applied to M1,M2 and M3,M4
- By turning M1,M2 and M3,M4 on and off, the RF signal is mixed to the intermediate frequency (IF)
- Advantages: LO and RF are both balanced, good port-to-port isolations, high intercept points
- Disadvantages: high LO level required, high power supply



Important performances and required analyses:

Mixer performance	Analysis (Cadence ADE)
Harmonic distortion	Periodic Steady State (PSS)
S-Parameters	PSS and Periodic S-Parameter (PSP)
Noise figure	PSS and PNoise
Conversion gain	PSS and Periodic Transfer Function (PXF)
Port-to-Port isolations	PSS and Periodic AC (PAC)
1dB Compression Point	Swept PSS
2nd/3rd order Intercept Point	Swept PSS
Power consumption	PSS or DC

Difficulties:

- no unique testbench, that fits for all performances
- different configuration of the analyses are required but not allowed within the same Artist session
- due to this limitation no full optimization of the mixer is available with IC5.1 and WiCkeD 5.0

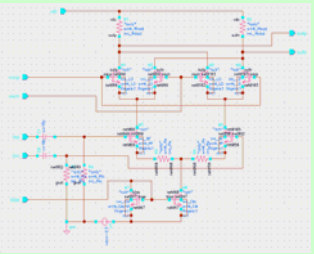
MunEDA DFM-DFY Tool Family WiCkeD

MunEDA offers numerous tools for circuit analysis, diagnosis and circuit optimization as well as interfaces to industrial standard and inhouse design environments and simulators.

Example circuit, initial sizing and simulation results

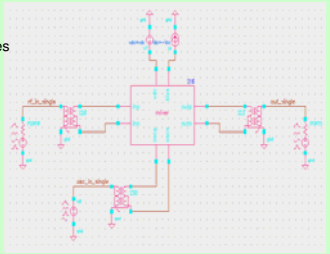
Example Circuit & Initial Sizing:

- CMOS mixer based on Gilbert Cell topology
- it consists of:
  - the Gilbert Cell
  - a current mirror
  - resistors and capacitors
- all NMOS transistors W=230u, L=600n (ex. M7)
- load resistors (R1, R2) W=3.5u, L=1u (500 Ω)
- source resistors (R3, R4) W=180u, L=1u (10 Ω)
- input resistors (R5, R6) W=1u, L=9.6u (10 kΩ)



Testbench:

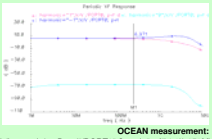
- The testbench consists of:
  - the mixer DUT
  - three baluns
  - ports and sources
- Frequencies
  - fRF = 2.5 GHz
  - fLO = 2.75 GHZ
  - fIF = 250 MHz
- Sources
  - vdc = 2.5 V
  - idc = 600 µA,
  - alo = 600 mV



Simulation results before optimization:

Conversion gain = 6.97 dB

- measured with PSS/PXF
- $f_{in} = f_{out} + k_i \cdot f_{PSS}$
- $f_{PSS} = f_{LO} = 2.75$ GHz
- k_i = -1 (lower sideband)
- $f_{out} = f_{IF} = 250$ MHz
- f_{in} = -2.5 GHz

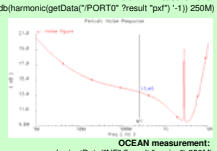


OCEAN measurement:
value(db(harmonic(getData("/PORT0" ?result "pxf") '-1)) 250M)

Noise figure = 13.45 dB

- measured with PSS/PNoise
- $|f_{in}| = |f_{out} + \text{refsideband} \cdot f_{PSS}|$
- $f_{PSS} = f_{LO} = 2.75$ GHz
- refsideband = -1
- $f_{out} = f_{IF} = 250$ MHz
- f_{in} = 2.5 GHz

Power consumption = 25.11 mW



OCEAN measurement:
value(getData("NF" ?result "pnoise") 250M)

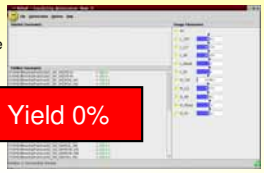
WiCkeD Contraint Setup, Analysis and Optimization Flow*

Step1 – WiCkeD Contraint Editor Settings:

- Design and Op. Parameters:
  - temp: from -20 °C up to 50 °C
  - vdc: from 2.4 V up to 2.6 V
- Constraints:
  - nSat for differential pair M5, M6 is disabled
- Performance specifications:
  - conversion gain > 8 dB
  - noise figure < 13 dB
  - power consumpt. < 50 mW

Step2 – Simulation & Feasibility Optimization:

- Simulation Results:
  - two performance specifications (conversion gain and noise figure) are not fulfilled
  - after a Screening the parameters L_Rin and W_Rin are removed due to less than 10% influence
  - 10% is freely chosen
- Feasibility Optimization
  - one violated contraint in the current mirror
  - optimization successful after two iterations

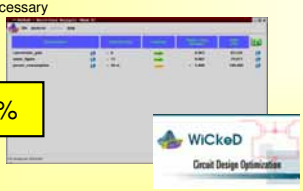


Step3 – Nominal Optimization:

- Conversion gain and noise figure are outside the specification bounds
- a previous sensitivity analysis showed that the L's of the differential pairs have the most influence on conversion gain and noise figure
- after one iteration the optimization is successful

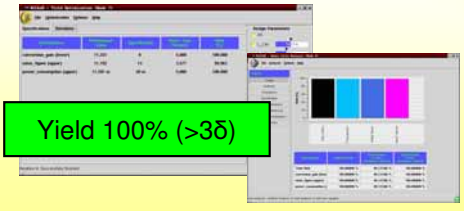
Step4 – Worst-Case Analysis:

- Yield after Nominal Optimization between 79% and 100%
- Improvement is neccessary

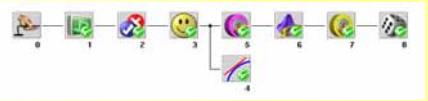


Step5 – Yield Optimization & Monte-Carlo Verification:

- Yield can be increased up to 100% (WCD > 3σ) after 4 iterations
- Monte Carlo Analysis confirms the results of the Yield Optimization



Results & Optimization Flow:



- Optimization of the CMOS mixer was successful
- All selected performances fulfill the specification
- Yield can be increased up to 100%
- Special RF analyses and OCEAN postprocessing functions can be used with WiCkeD
- The complete characterization and optimization of a mixer circuit requires multiple testbenches/multiple analyses of the same type

MUGM07

***) Results published at MUGM2007**

Dr. Manfred Dietrich, Head of Department Mixed-Signal Systems, Fraunhofer IIS EAS:
"With WiCkeD all selected performances have fulfilled the specifications. The yield of the analyzed and optimized CMOS mixer circuit could be increased up to 100%."

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