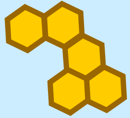


2A713 HONEY

Highly Optimized Design Methods for Yield and Reliability

Motivation

Technology push

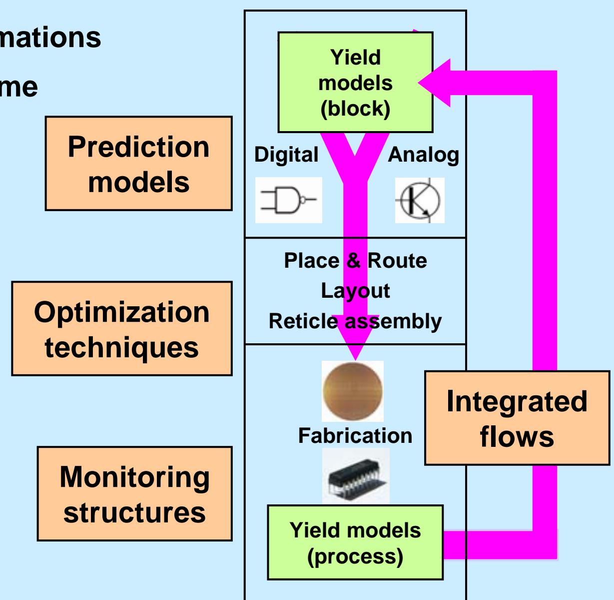
- For the 65 nm node and below, higher process variations lead to a strong increase in parameter dispersion
- IC features are getting far smaller than the wavelength of light. This creates optical distortions from layout to lithography
- Reliability effects and more sensitive circuits due to reduced supply voltage will close the design window in 65nm and below

Application pull

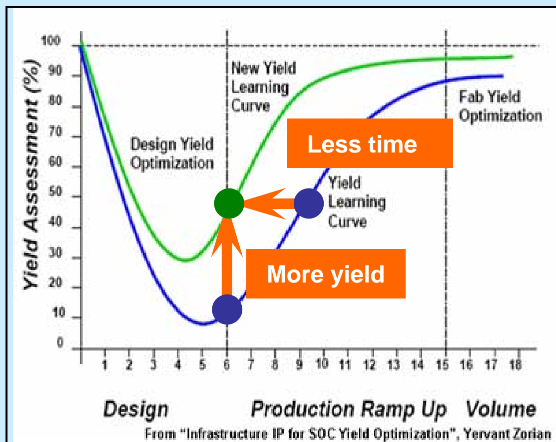
- Emerging mixed-signal applications (such as RF) have a higher sensibility to parametric yield loss
- New markets are appearing with more demanding reliability requirements, i.e. transportation, medicine (intelligent implants for individual drug delivery…)

Targeted metrics

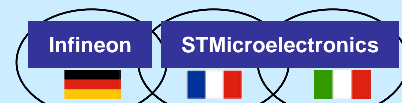
- Provide early yield & reliability estimations
  → Right volume at right time
- Counterbalance yield decrease
  → Cost effectiveness
- Define a trade-off between yield, reliability and performances
  → Circuit quality



Addressing yield and reliability at different steps of the design flow



Yield optimization at design time will provide a positive impact during production ramp



HONEY: a cooperation between 2 big European players and their partners

HONEY in brief

- **Structure :** 1. Block and circuit design
  2. Automated layout/reticle generation and optimization
  3. Process maturity monitoring through predictions and measurements
- **Duration :** 07 / 2007 - 12 / 2010
- **Manpower :** 180 man.year
- **Countries :** France - Germany - Italy
- **Partners :** Dolphin (F), IMEP (F), IMMS (D), Infineon (D), InfiniScale (F), MunEDA (D), ST (F & I), X-Fab (D), Xyalis (F)
- **Contact :** Philippe.Garcin@st.com

DOLPHIN INTEGRATION · imep · IMMS · infineon · infiniscale · MunEDA · ST · X-FAB · XYALIS