

Robust Analog Design for Automotive Applications by Design Centering

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Abstract

The effects of random variations during the manufacturing process on devices can be simulated as a variation of transistor parameters. Device degradation, due to temperature or voltage stress, causes a shift of device parameters, for example threshold voltage V_{th} , which can also be modeled as a degradation of transistor parameters. Therefore, in order to design circuits, which are robust and reliable, analysis and optimization of their sensitivity to variations in model parameters is important. Furthermore, constraints on the operating regions and voltage differences of transistors are used in order to keep operating points stable over a large temperature range. In this work, using three circuits for automotive applications and current process development kits (PDK), we show how design centering software can be used to consider both sensitivity reduction towards model parameter variation and constraints to control safe operating areas (SOA).

1 Introduction

Design for reliability stands for design methods, which reduce the degrading effects on device level and on metallization level, as well as for implementing design techniques to tolerate a reasonable amount of degradation [1]. Many different reliability issues are to be considered in the sub-90nm era for both interconnects and devices. Among the interconnect reliability issues are for example electromigration, stress-induced voiding and power grid voltage drop (IR - drop). Device reliability issues include gate oxide breakthrough, negative bias temperature instability (NBTI) and hot carrier stress (HC). Statistical process variations of device parameters are often considered to be a device reliability issue, although it is not a stress-induced degradation of the circuit during its lifetime, but is caused by variations in the manufacturing process. Design-for-Yield (DfY) has to consider statistical process variation on a device level, too, but does not consider device degradation after the manufacturing.

Statistical process variation, HC and NBTI all have in common that they cause a soft degradation of device parameters such as V_{th} . On a circuit level, this can cause a soft (parametric) fault, i.e. the circuit is still functional but violates its specification, for example maximum offset or minimum gain. This may cause more severe violations of the specification at higher levels in the design hierarchy.

In the sub-90nm era, device sensitivity towards HC and NBTI must be considered during technology development. Statistical process control (SPC) is used extensively during manufacturing to keep variations under control. Layout design rules and DFM methods help to avoid local defects. Nevertheless, the remaining variations can cause a significant parametric yield loss for an increasing number of de-

signs if they are not considered and safeguarded against by circuit design.

For many analog circuits, the impact of device parameter variation on the performance figures at circuit level is usually not obvious and depends on the chosen circuit topology, sizing, operating point and type of performance.

To actually simulate the device degradation caused by HC and NBTI, reliability models have been developed [2]. Their model parameters must be extracted in addition to the usual device model generation. Circuit simulation to calculate device degradation can then be carried out in a sequence of simulation steps controlled by special tools [3]. Although they have been a topic of research for nearly two decades, these reliability models and corresponding simulation techniques are not yet widely available in current PDKs and design flows. The situation is different for statistical process variation, with current PDKs usually containing statistical information used by standard industry simulators to run Monte Carlo simulation. As such, it is a realistic and interesting question, how to consider sensitivity towards device degradation and avoiding device stress situations, without having reliability models and corresponding simulation techniques at hand.

In this paper, we explain a design centering technique, which reduces the sensitivity of a circuit's performance towards changes of device parameters, in combination with electrical constraints on operating conditions. Existing degrees of freedom for sizing are used to find the sizing, which is least sensitive towards variation of device parameters while avoiding conditions that may lead to increased device stress. We further discuss how existing methods for design centering have to be enhanced to include results from reliability simulation for technologies where such models exist and can be used by the designer for reliability simulation.

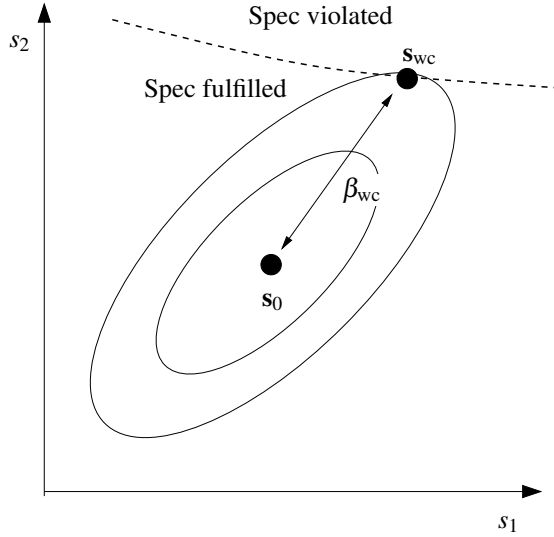


Figure 1: Definition of worst-case point.

2 Design Centering

In order to simulate statistical variation and device degradation, model parameters of the transistor model are varied, e.g., threshold voltage V_{th} or mobility μ_0 . Note that electrical characteristics such as max. I_{ds} or transconductance g_m are simulation results, which depend on the operating conditions, but are not parameters of a transistor model like BSIM. All such variable model parameters are collected in the parameter vector \mathbf{s} . Another set of parameters is the vector \mathbf{d} of design parameters, such as the width or length of the transistors. These parameters can be set by the designer in order to improve the performance and robustness of the circuit.

After production, model parameters are assumed to be Gaussian distributed with a mean vector \mathbf{s}_0 and a covariance matrix \mathbf{C} .

The yield Y is the percentage of circuits which fulfill the specifications. A specification is a lower bound on a performance, for example slew rate $SR \geq 3V/\mu s$. If we denote each individual specification with $f_i(\mathbf{s}, \mathbf{d}) \geq b_i$, then the set of process parameters that fulfills a specifications i is

$$A_i(\mathbf{d}) = \{\mathbf{s} | f_i(\mathbf{s}, \mathbf{d}) \geq b_i\}, \quad (1)$$

with a similar definition for upper bounds. The set of process parameter vectors that fulfills all specifications is the acceptance region

$$A(\mathbf{d}) = \bigcap_i A_i(\mathbf{d}). \quad (2)$$

The parametric yield Y_i is the percentage of circuits that fulfill the specification i :

$$Y_i(\mathbf{d}) = \int_{A_i(\mathbf{d})} |2\pi\mathbf{C}|^{-\frac{1}{2}} \exp\left(-\frac{1}{2}(\mathbf{s}-\mathbf{s}_0)^T \mathbf{C}^{-1}(\mathbf{s}-\mathbf{s}_0)\right) ds \quad (3)$$

where the argument of the integral is the probability density function of the multinormal distribution. The total yield $Y(\mathbf{d})$ is the same integral over A instead of A_i .

Figure 1 shows the mean value, covariance ellipsis and one specification bound in process parameter space. Of all

process parameter sets which violate a specification i , the point that is closest to the mean value is called the *worst-case point* \mathbf{s}_{wc} . It marks the position in the process parameter space where the probability density of parametric faults has its maximum. The distance between \mathbf{s}_{wc} and \mathbf{s}_0 is the *worst-case distance*

$$\beta_{wc} = \sqrt{(\mathbf{s}_{wc} - \mathbf{s}_0)^T \mathbf{C}^{-1}(\mathbf{s}_{wc} - \mathbf{s}_0)} \quad (4)$$

Due to device degradation during operation, the mean value and the covariance matrix of the circuits change with time t : $\mathbf{s}_0(t)$, $\mathbf{C}(t)$. Therefore, the percentage of circuits that still fulfill their specification at time t is

$$Y(\mathbf{d}, t) = \int_{A(\mathbf{d})} |2\pi\mathbf{C}|^{-\frac{1}{2}} \exp\left(-\frac{1}{2}(\mathbf{s}-\mathbf{s}_0(t))^T \mathbf{C}^{-1}(\mathbf{s}-\mathbf{s}_0(t))\right) ds \quad (5)$$

If we consider the influence of process variation on the sensitivity towards stress-induced degradation as a second order effect, then we may assume $\mathbf{C}(t)$ to be constant. The effect of degradation during operation on the yield is then formally similar to a process drift during manufacturing (see figure 2). The initial values after production at $t = t_0$ are $\mathbf{s}_0(t_0)$.

For small changes in the position of the mean value, the change of worst-case distance over time is

$$\beta_{wc}^{(i)}(t) = \beta_{wc}^{(i)}(t_0) - (\mathbf{s}_0(t) - \mathbf{s}_0(t_0))^T (\mathbf{s}_{wc}(t_0) - \mathbf{s}_0(t_0)) / \beta_{wc}^{(i)}(t_0) \quad (6)$$

This change can be positive or negative, i.e. a performance can become better or worse by device degradation.

In order to resist process drift and device degradation, it is not sufficient to optimize only the yield figure $Y(\mathbf{d}, 0)$, because this value goes into saturation at 100%. Standard methods for the estimation of Y , which means counting Monte Carlo samples, are not accurate enough to estimate the worst-case distance. A robust and a non-robust design may show the same yield value $Y(\mathbf{d}, 0)$, but different worst-case distances, which means different sensitivities towards

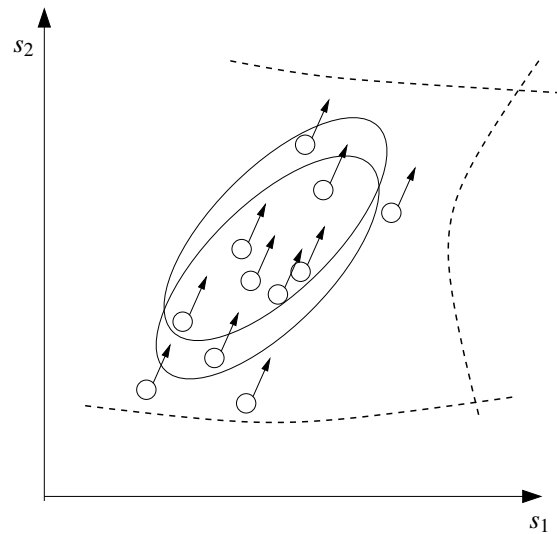


Figure 2: Process drift or device degradation.

process drift or device degradation. Optimization for yield and robustness, therefore, has to focus on the worst-case distances as the primary targets for optimization of robustness and yield [4].

As a result, this advantage of worst-case distance optimization in contrast to optimization of Y becomes even more important for the design of robust and reliable analog circuits. The combination of worst-case distance optimization and SOAs is the basis of our approach. The SOAs can be formalized as functions of the design parameters, which impose further constraints on the optimization problem:

$$\mathbf{c}(\mathbf{d}) \geq 0. \quad (7)$$

During the worst-case distance optimization, design points are accepted as valid, only if they fulfill all such constraints. The solution has to show high worst-case distances for each performance f_i , while satisfying all constraints $\mathbf{c} \geq 0$.

3 Physical SOA Motivation

Device reliability is becoming more and more important within circuit design. For designers, a more general definition of a safe operating area (SOA) is of interest here. This area is defined as the voltage and current conditions over which the device can be expected to operate without self-damage. Based on this SOA definition we turned our interest to the following four issues:

- a) Substrate current,
- b) Operating temperature,
- c) Channel heating, which is caused by the Joule energy of the device, and
- d) Design optimization.

Particularly automotive applications demand high chip device reliability under extreme operating conditions. We understand design for automotive applications to assure defined functionality and chip performance under a wide temperature range. In this case it means that chips must work under high temperature conditions, i.e. at about 150°C.

Thus one of our first intentions, which regard to device reliability, was concentrated on substrate current, which can be used as an integral monitor of process quality [5]. In this context we worked on design methods to additionally eliminate minority carriers in order to suppress uncontrolled substrate currents [6]. Later on, we optimized the design of these structures to realize an absolute prevention against latch up of CMOS structures under automotive conditions [7]. As a result, the design measure developed allows trigger currents of parasitic four-layer bipolar structures as high as 400mA at 150°C. Such parasitic bipolar structures cannot be avoided within a standard CMOS technology.

Furthermore, it is known that the intrinsic carrier density within silicon [8] doubles for every eleven temperature degrees. Another point of view is demonstrated by A. M. Abo [9] By analyzing the breakdown and degradation phenomenon in MOS devices, he was able to show that relative

terminal potential determines device lifetime. Taking into account the heating-up caused by high power density [10] at electric field maximums, it is ultimately the high operating temperature, which poses a design challenge.

Additional evidence of the major influence of high temperature on chip reliability can be taken from the Arrhenius relationship. The Arrhenius relationship, which is common in many physical and chemical processes, has also been found to fit failure rates in ICs [11]. Figure 3 shows the failure rate over temperature for two activation energies. Based on élantecs analysis, the failure rate, for instance for an activation energy of 1.0eV, is 100,000 times larger at a junction temperature of 150°C than it is at 30°C.

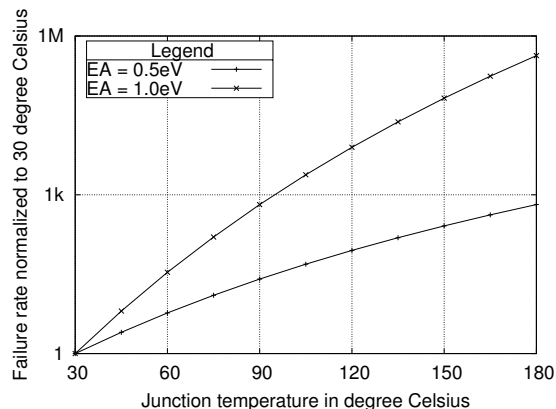


Figure 3: Failure rate vs. junction temperature [11].

Usually, design for reliability (DFR) of a chip identifies design features which are potentially vulnerable to various physical effects, which can in turn degrade circuit performance. This is similar to design for yield and manufacturing (DFY/DFM). For now our attention is not directed at estimating the degree of reliability by simulation. Current methods and tools are focused on reducing the sensitivity of the performance parameters to design, process and operating parameters [12]. Such an approach corresponds quite well with the three design steps proposed by G. Taguchi [12]:

1. System design
2. Parameter design
3. Tolerance design

In addition to the definition of functional constraints, we will now introduce reliability constraints. This procedure becomes obvious for the saturation voltage. Here the functional constraint defines the lower limit of the saturation voltage and the equivalent reliability constraint on the contrary defines the upper limit of the related saturation voltage. An example of this methodology is shown in section 4, regarding the so called self regulating cascodes (SBC), where we limit the maximum drain source voltage of the main transistor, which in turn drives the maximum current.

Moreover, together with the development of an 0.18µm Automotive CMOS technology, we are also working on a method to predict our product reliability. The future goal is to predict the long term performance of our designs.

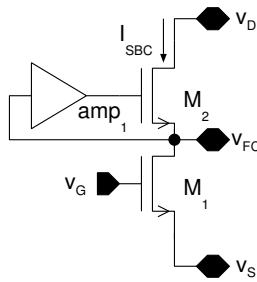


Figure 4: Equivalent circuit of self-biasing cascodes (SBCs).

4 Safe Operating Area Constraints

Constraints on circuit design to reduce device stress are based on current density. The documentation of our current PDKs give the analog designer information about

1. Maximum voltage difference
2. Maximum path current
3. Safe operating area

for every device [13].

Device voltage differences and device absolute node voltages can be checked and specification violation can be traced into a log file. This can be realized at model level. One possible way to achieve this is using verilogA-capsuled models.

A minimization of the voltage difference is suggested for high current paths. Special circuit topology and optimization can help to realize this. Figure 4 shows a practical example.

Due to the application of the SBC structure inside an amplifier (see section 5.1), high current load is possible inside the branch v_D to v_S . Stress of the most critical device M1 can be limited by defining the drain-source voltage v_{ds} of the device upside and close to the saturation voltage v_{dsat} . For this

	geometrical	electrical
function	$L_1=L_2$	$V_{gs}-V_{th} > V_{invmin}$ $V_{ds} - (V_{gs} - V_{th}) > V_{satmin}$ $ V_{ds,1}-V_{ds,2} < V_{dsdiffmax}$
robustness	$L > L_{min}$ $W > W_{min}$ $L*W > A_{min}$	
reliability		$V_{ds} - (V_{gs} - V_{th}) < V_{satmax}$

Figure 5: Overview of constraints for the SBC circuit.

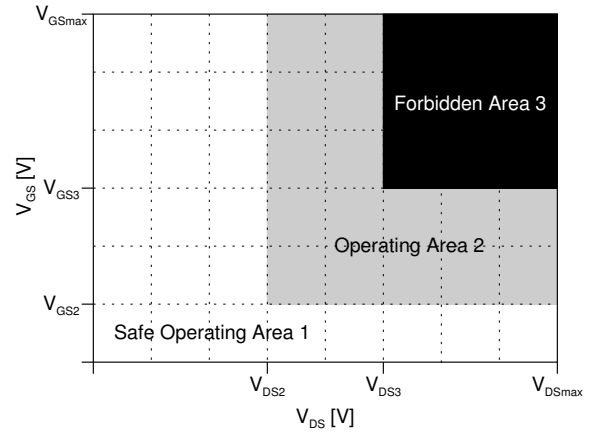


Figure 6: SOA diagram.

purpose an active control stage was integrated to improve the cascode properties and to limit the drain-source voltage of M1 certain milli volts above the saturation voltage v_{dsat} . A constraints classification for this example used within the optimization regarding reliability is presented in figure 5.

SOA diagrams give additional parameters in general about special devices (see figure 6). Such rules are used during circuit design using power and high voltage devices. The mathematical formulation of the rules can be prepared by PDK or designer. WiCkeD [14] supports structure constraints and performance constraints which are considered during the analysis and optimization. In general, the PDK has to contain templates for structural constraints which allow automatic constraint generation. The designer can add other performance constraints manually. The example in figure 7 shows constraints for a special high voltage device.

	geometrical	electrical
function		$V_{gs}-V_{th} > V_{invmin}$ $V_{ds} - (V_{gs} - V_{th}) > V_{satmin}$
robustness	$L > L_{min}$ $W > W_{min}$ $L*W > A_{min}$	
reliability		$V_{ds} < V_{dsmax}$ $V_{gs} < V_{gs2}$

Figure 7: Constraints for special devices (see figure 6).

5 Examples and Results

The next three examples were realized using ZMD's $0.6\mu\text{m}$ automotive CMOS technology [15]. The current features of the PDK were used to consider reliability issues during the design and optimization phases. Sensitivity reduction and SOA rules, as described above, were used to design robust and reliable circuits.

5.1 Complex Operational Amplifier

The first example for automotive applications is an operational transconductance amplifier (OTA) for a 14 bit cyclic redundant signed digit (RSD) analog-digital converter (ADC). Figure 8 shows the simplified schematic of the realized OTA [16]. As a special measure, we replaced simple cascodes of a common OTA structure with self-biasing cascodes (SBC) to realize the demanded high dc gain, which was based on earlier design analyses [17, 18].

The trade off between dc gain higher than 110dB and settling time faster than 100ns could be solved for driving a capacitive load of 3pF – 9pF over the automotive temperature range from -40°C up to 150°C . In the literature, you will only find solutions for smaller temperature ranges, e.g. [19].

Design centering and further analyses with WiCkED tool features, such as mismatch and sensitivity analysis [14] were used. The results are shown in table 1 and a chip photo in figure 9.

Besides the built-in constraints of the WiCkED tool, we found essential constraints to guarantee the function and to reduce the stress of the devices (cf. figure 5). Saturation constraints were defined to ensure SBC's functionality of high output resistance. Constraints to control device stress are

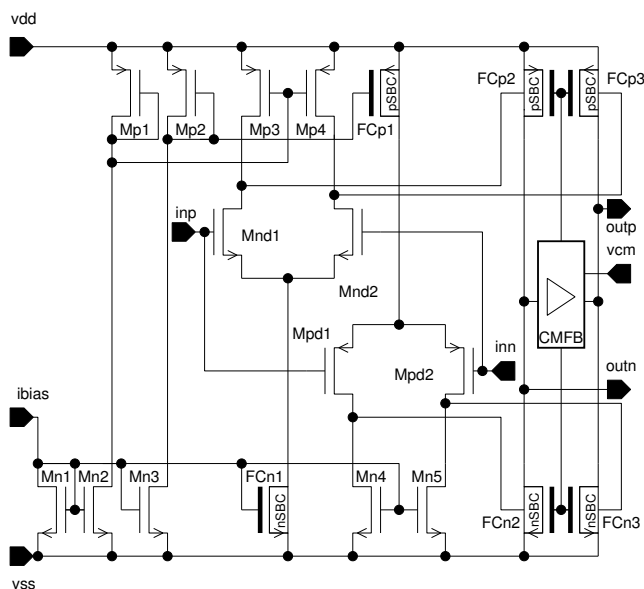


Figure 8: Simplified schematic of the fully differential folded cascode OTA.

CMFB: common mode feed back, nSBC: n-channel self-biasing cascode, pSBC: p-channel self-biasing cascode

Performance	Value	Comment
DC Gain	>110dB	
GBW	>50MHz	
Settling time	<100ns	error < 0.01%
Area	$300 \times 300 \mu\text{m}^2$	$0.6\mu\text{ CMOS}$
Supply current	$\approx 2.5\text{mA}$	@ 5V
Yield prediction	$\approx 98\%$	

Table 1: Performances of the OTA with key parameters. Operating range: temp: -40°C up to 150°C , capacitive load: 3pF up to 9pF, power supply: $5 \pm 0.5\text{V}$.

voltage differences inside the SBCs which are called SOA constraints in this paper.

5.2 Current Reference

Current supply concepts for analog blocks are based on current references in general. The main schematic of a current reference is shown in figure 10. It is also known as a V_T -referenced bias circuit and commonly used in CMOS technologies where the bipolar transistors are parasitic devices.

The function and design of such basic blocks are described in detail in [20, 21]. The feedback loop forces the same bias current of both bipolar transistors Q_1 and Q_2 . These transistors differ by the factor $n = m_{Q1}/m_{Q2}$. Hence a difference

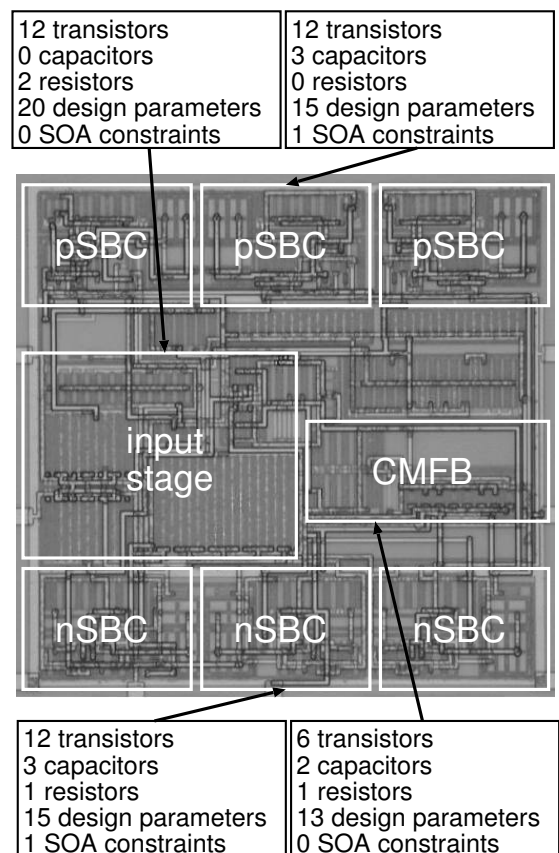


Figure 9: Chip photo of the realized OTA.

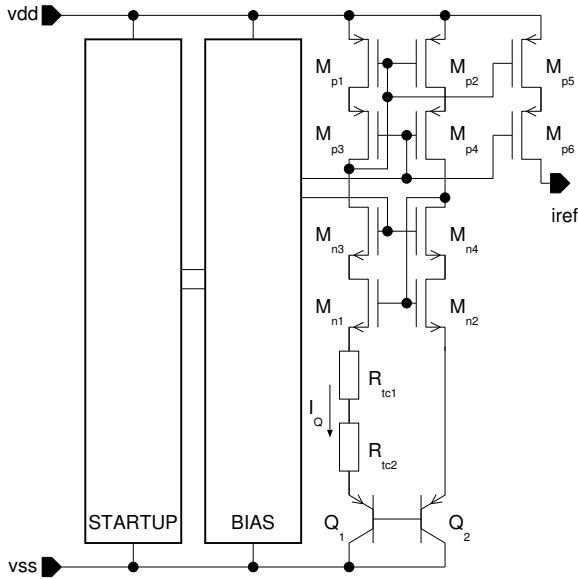


Figure 10: Core of the current reference.

in the two base-emitter voltages can be seen across the resistors. The temperature dependency of the current I_Q depends on the bipolar transistors as well as the resistor. To get a smaller temperature coefficient the resistor is realized as a combination of two single resistors using positive and negative temperature coefficients:

$$I_Q(T) = \frac{V_T \ln(n)}{R(T)} \quad \text{with} \quad R = R_{tc1} + R_{tc2} \quad (8)$$

The variation of the reference current of the initial design (cf. table 2) fails the specification $i_{ref} = 10 \pm 20\%$. At this point it was not clear if an optimization of the circuit would pass the specification, or whether additional topology actions, such as trimming, would be necessary. We followed a systematic flow to improve the circuit as described in [22]. For a fixed set of the factor n , a design centering of the resistor and the feedback loop parts was carried out. The design centering step of WiCkeD's optimization flow [14] was the important step (see table 2) towards improving the circuit's performance. The resulting temperature coefficient of the resistor pair was adjusted and the mismatch sensitivity of the NMOS transistors M_{n1-4} threshold voltages could be

Performance	Design	
	initial	centered
Yield	90%	100%
Worst Case Distance	1.2σ	3.7σ
CPK	0.5	1.4
Area	$180 \times 140 \mu\text{m}^2$	$180 \times 180 \mu\text{m}^2$

Table 2: Performances of the current reference $i_{ref} = 10 \mu\text{A} \pm 20\%$. Operating range: temp: -40°C up to 165°C , power supply: $5 \pm 0.5\text{V}$.

reduced. The second improvement item required additional area (see table 2), but it consumed less effort as a trimming solution. This action would comprise additional parts such as a trimming network and an EEPROM. For the optimized circuit this action is only advisable if a more ambitious specification is used.

5.3 Hierarchical Analog Block

LIN transceiver ICs are a standard product within the ZMD portfolio [23]. LIN (Local Interconnect Network) is a low cost serial communication system intended to be used for distributed electronic systems in vehicles [24]. The communication is based on the SCI (UART) data format, a single-master/multiple-slave concept, a single wire 12V bus and a clock synchronization for nodes without a stabilized time base.

Figure 11 shows the simplified LIN interface block of the bus line driver and receiver (transceiver), which is configured as an IP cell. Inverse polarity protection and a pad stage are also part of the block. Besides the voltage and current supply (not shown in figure 11), a high voltage supply V_{board} and a current reference i_{ref} have to be applied for application.

The interface converts the digital transmission signal txd to the analog 12V LIN bus signal. Thereby the slew rate control stage forms the rising and falling edge and the output stage drives it to the LIN bus. The performance parameter, e.g., slew rate $SR = 0.5\text{V}/\mu\text{s} \dots 3\text{V}/\mu\text{s}$ and symmetry of transmitter propagation delay $SYM = \pm 2\mu\text{s}$ at the LIN bus, are specified with close tolerances. In the opposite direction, an analog signal at the 12V LIN bus is converted in the input stage into the digital receive signal rxd . Both the transmitting and receiving procedures use the same pad stage.

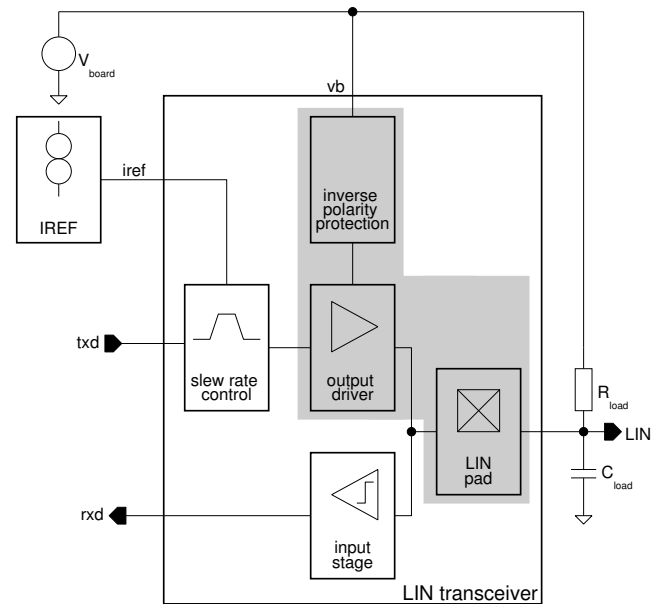


Figure 11: Block view of the LIN transceiver IP cell. Low voltage and current supply not shown. SOA rules have to be checked inside the grey marked blocks.

Design	Main Step	Description	Tool
OTA	A	Feasibility of main topology	FO, NO
	B	Optimization of the SBC sub-blocks	FO, NO, MC
	C	Optimization of main circuit	FO, NO, WCO
	D	Yield analysis and optimization	MC, WCD, MM, YO
	E	Final centering, rounding and verification	YO, MC, WCA
IREF	A	Optimization of main circuit	NO, YO
	B	Search mismatch pairs to reduce deviation	MM
	C	Final centering, rounding and verification	YO, MC
LIN	A	Search sensitive blocks and devices	PS, ST
	B	Optimization of the slew rate control block	NO, YO
	C	Final centering, rounding and verification	YO, MC

Table 3: Main design steps of each example.

Key: FO Feasibility Optimization, NO Deterministic Nominal Optimization, WCO Worst Case Operation Analysis, MC Monte Carlo Analysis, PSC Parameter Screening, ST Sensitivity Analysis, WCA Worst Case Analysis, WCD Worst Case Diagnosis, MM Mismatch Analysis, YO Yield Optimization.

The verification of the initial design using our in-house verification environment called *zmdAnalyser* [25] showed problems in the parameter slew rate symmetry *SYM* at one automotive operating condition. First a sensitivity analysis and parameter screening were used to isolate the problematic part (see table 3) of the hierarchical design, which contains approximately 300 devices. The slew rate control block and its current bank stage (not shown in figure 11) could be initially extracted as critical parts. However, a single verification of the slew rate control and the current bank block showed that the blocks cannot be treated separately and the blocks of the complete transmit signal path also have to be considered, including the high voltage part. Further main steps of the circuit improvement are given in table 3. The design centering step was used to reduce the sensitivity of the design to the global process deviation and was carried out using *WiCkeD* [14].

In this case, the high voltage stage of the LIN transceiver was not part of the optimization process. To ensure the reliability of the high voltage devices, the PDK provides conventional SOA rules. SOA diagrams were used to design the high voltage stage. Node voltage limits were derived from the SOC diagram and used within the verification step. Finally SOA constraints were applied for checking (see table 7). The SOAs were realized as calculator expressions. So the expressions can be used for both tools *WiCkeD* and the *zmdAnalyser*.

The final results of the optimization are given in table 4. The column "design centered A" contains the results after the slew rate block optimization. The right column, labeled "design centered B", presents the results when only the current reference block is replaced by the optimized block discussed

above. This example shows that centered blocks can be advantageously combined in an IP cell concept design.

Performance	Design		
	initial	centered A	centered B
Yield	71%	95%	95%
WorstCaseDistance	0.56σ	1.64σ	1.66σ
Additional Area	—	$80 \times 80 \mu m^2$	$180 \times 40 \mu m^2$

Table 4: Performances of the LIN transmitter with the parameter symmetry = $\pm 2\mu s$. Operating range: temp: $-40^\circ C$ up to $140^\circ C$, low voltage supply: $5 \pm 0.5V$, high voltage supply: $6.5V-18V$.

6 Summary and Outlook

In this paper we have shown, how reliability issues of current PDKs can be taken into account by using *WiCkeD*, using three practical design examples for automotive applications. At this point, design centering is used to decrease the sensitivity of parameter changes and to check SOA constraints.

Even though the design effort directed at higher reliability includes a set of measures such as handling substrate currents the design centering is the key to improving the yield.

The use of SOA methodology is a way of ensuring reliability. The combination of both yield improvement and consideration of SOA constraints is one key to designing robust and reliable circuits.

In this context, besides the substrate current and future prediction of long term reliability via simulation, our main

attention is focused on the influence of high temperatures on parameter change.

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