Yield Optimisation of Power-On Reset Cells and Functional Verification

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Abstract

Simulation based yield optimisation is becoming an important solution for increasing robustness of analog IP blocks. This paper describes the yield optimisation of a power-on reset cell as part of an analog IP library. Yield analysis of the initial design is performed and sensitivities with respect to process parameters are determined by Monte Carlo simulation. The input parameters used for the Monte Carlo simulation describe global and local variations of the semiconductor devices. The results of the yield analysis are used to determine a shift of the PMOS threshold implant dose enabling a yield enhancement of the initial design. A re-design using simulation-based design centering is performed resulting in a significant yield increase in consideration of the operating conditions. The optimisation is based on an algorithm maximizing the worst-case-distance. The simulation results on improved production yield are verified by electrical test at wafer level for varying process conditions.

1 Introduction

The performance and the yield of analog circuits are determined by variations of the production process. During the development of analog building blocks (e.g. band gap cells, operational amplifiers, comparators etc.) the designer chooses a circuit topology and tries to achieve a given nominal target for a pre-defined performance vector. Afterwards it must be verified that the design is functional under varying process and operating conditions (e.g. supply voltage and temperature variation). To calculate the yield of a circuit dependent on both global and local variations, Monte Carlo simulation is supported for most CAD platforms [1]. A critical point with respect to the accuracy of Monte Carlo simulation is the accurate statistical modelling of the SPICE parameters reflecting the distribution of basic process parameters (e.g. threshold voltage, gain factor or channel length). Methods for accurate determination of Monte Carlo parameters from electrical test data are presented in [2,3]. The distribution of global process parameters is determined from the statistics of the relevant process control parameters and correlations of the parameters should be taken into account. The distribution of local fluctuations (mismatch) is determined from statistical parameter extraction of measurements on special test chips [4,5]. Besides the information on the yield of the circuit with respect to a given specification it is also important to get information about the main contributors of yield loss by means of sensitivity analysis with respect to design and process parameters. This information can be used in two ways. First, for a nominal design having a low yield at some operating corner, the designer can shift design parameters of the relevant devices (main contributors) enabling efficient design centering [6,7,8] during a re-design phase. Secondly, during product ramp up the sensitivity analysis gives information about possible process shifts to increase the yield of the original design. Design for Yield (DFY) tools provide both sensitivity analysis and yield optimisation based on Monte Carlo simulation. Simulation based yield optimisation is performed by design centering and automatic shift of design parameters within specified design parameter limits. In the present investigation the yield of an analog building block (power-on reset cell) is increased by two ways: first a shift of production parameters is calculated from sensitivity analysis to increase the yield of the initial design and afterwards a new set of design parameters is determined by maximizing the worst-case-distance (sigma to target) for the reset voltage. The simulated yield increase is verified by production results using process window verification.

2 Problem Formulation and Circuit Description

A power-on reset cell has been used as an IP block within a mixed-signal circuit and has been designed using a standard 0.8µm CMOS technology. During yield ramp-up of the product it turned out that there is significant yield loss at low temperature (-40°C). The yield loss could be attributed to the threshold voltage V_{TRIG} of the power-on reset cell which was measured during electrical wafer test. Therefore it was decided to perform a yield analysis of the circuit pursuing two goals: First, find a possibility to shift the production process in order to increase the production yield of the current design and afterwards find a new set of design parameters using the given circuit topology (see Fig. 1) that will result in a improved yield over the whole temperature range (-40°C to 85°C) without changing the process.

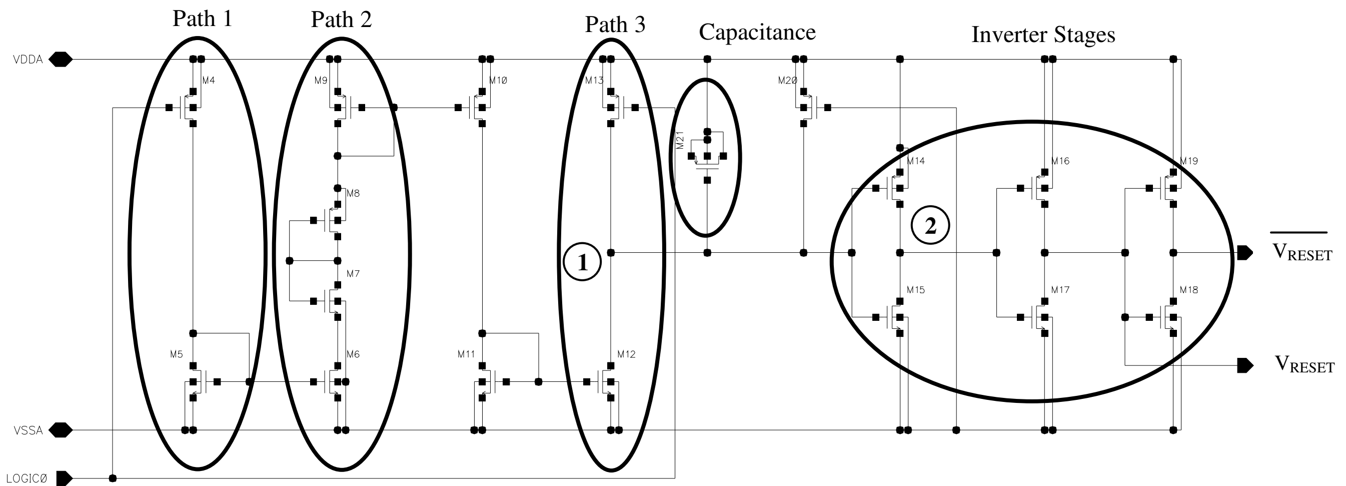

Fig. 1. Schematic of the Power-On Reset Cell

The Power-On Reset cell is used to reset the outputs of digital gates. When the supply voltage reaches the threshold voltage level V_{TRIG} the output of the cell V_{RESET} switches to low. The level of the threshold voltage is mainly defined by the voltage drop at the transistors in Path 2 and with this path the currents of the current sources M4 and M13 are compared. To explain the main function of the cell two different supply sources considering the rise time have to be distinguished:

1) Slow Rise Time (s)

Figure 2 shows the simulated transient reset voltage V_{RESET} at room temperature (27°C) when a supply ramp with a constant slope of 5 V/s is applied. At the beginning of the transient examination the transistor M4 causes a current flow in Path 1 (see Figure 1). The transistor M13 causes the voltage level at Node 1 to rise with the supply voltage. The voltage level at this node is amplified by two inverters resulting in the reset voltage V_{RESET}. Therefore V_{RESET} rises in the same way as the supply voltage.

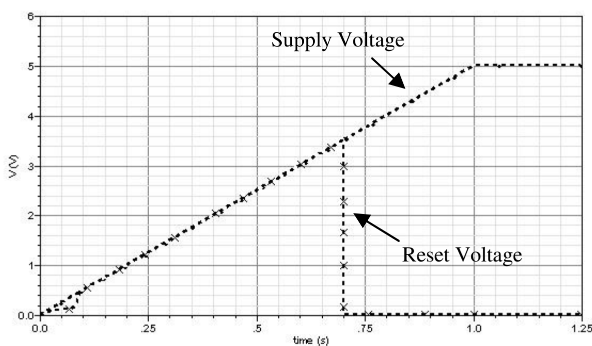

Fig. 2. Transient characteristic of the reset voltage V_{RESET} for a supply voltage with a slow rise time

The voltage level at Node 1 rises until a current can flow in Path 2. This current is mirrored by the transistors M9, M10 and finally by the transistors M11, M12 with a factor of 3. Thus a current flows in Path 3 and causes the voltage level at Node 1 to decrease. After the voltage level at Node 1 reaches a certain value (supply voltage reaches threshold voltage level V_{TRIG}) the first inverter (M14, M15) delivers a HIGH (corresponding to the value of the connected supply voltage) at its output (Node 2). This signal is inverted again by a second inverter (M16, M17) and delivers therefore a LOW (0V) at the reset output V_{RESET} of the Power-On Reset Cell.

2) Fast Rise Time (µs)

Figure 3 shows the simulated transient reset voltage V_{RESET} at room temperature (27°C) when a supply ramp with a constant slope of 10 V/µs is applied. Because the supply voltage is rising very quickly the Power-On Reset is not able to pull down the voltage level a Node 1 fast enough. Therefore the output V_{RESET} does not switch to zero at the defined threshold voltage V_{TRIG}, but when the supply voltage is already at the maximum value. To prevent short pulses (spikes) at the output of the cell the RC-element consisting of the transistors M21 (Capacitance) and M12, M13, M20 (Conductance) lengthens the pulse duration at the output V_{RESET}.

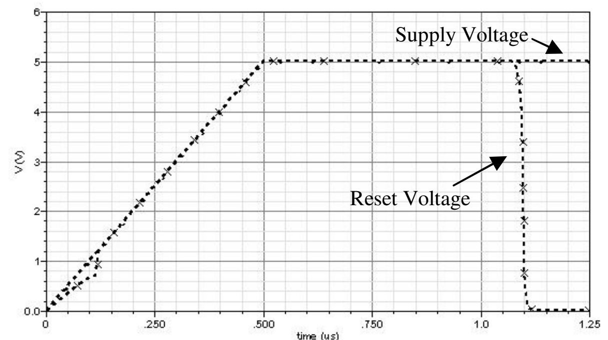

Fig. 3. Transient characteristic of the reset voltage V_{RESET} for a supply voltage with a fast rise time

3 Yield Analysis and Yield Enhancement

3.1 Monte Carlo Simulation

The variation of process parameters is derived from the statistical distribution of electrical test parameters for MOS transistors and mapped to the variation of SPICE parameters used for Monte Carlo simulation. The global and local variation of SPICE parameters in the Monte Carlo models are defined in the following way (e.g. for the MOS transistor threshold voltage vth0):

$$vth0 = vtnom + delvt + delmat \cdot \frac{A_{VT,sim}}{\sqrt{w \cdot l}} \quad (1)$$

where *vtnom* is the normally distributed nominal threshold voltage, $deltvt \sim N(0,\sigma_{VT})$ is a global random variable describing the process variation (wafer to wafer variation), *delmat ~ N(0,1)* is a local Gaussian random variable describing device mismatch and is allowed to vary independently for any transistor, *w* and *l* are the drawn width and length of the transistor. The third term of the parameter definition describes the geometric dependence of mismatch corresponding to the Pelgrom law [9], where the slope factor $A_{VT,sim}$ is determined from matching parameter extraction [4,5]. The distribution functions for the PMOS transistor threshold voltage variation corresponding to (1) are defined in Table I.

TABLE I

Monte Carlo modeling of PMOS threshold voltage variation.

vtnom [V]	**delvt** [V]	**delmat** [V]	$\mathbf{A_{VT,sim}}$ [mVµm]
- 0.76	N(0,0.03)	N(0,1)	15

In order to model the process variations accurately the following SPICE parameters for the MOS transistors (BSIM3v3) have been defined by random variables derived from the distribution of production control parameters: *vth0* (threshold voltage), *u0* (mobility), *xl* (variation of effective channel length), *xw* (variation of effective channel width), *nsub* (substrate doping), *tox* (oxide- thickness), *cgd/s/bo* (gate-drain/source/bulk overlap capacitances), *rsh* (diffusion resistance) and *cj* (junction capacitance). The calculation of the SPICE parameter distribution uses a backward error propagation method similar to [3] to model the variation of process parameters based on SPICE simulation of control parameters and numerical computation of sensitivities. Furthermore, correlations of SPICE parameters are defined reflecting the statistical interaction of process control parameters. The Monte Carlo models are implemented as special device model sections for usage within the SPICE simulator Spectre [1] and the DFY tool WiCkeD [6,7,8,10]. The yield analysis of the power-on reset cell is performed using the Monte Carlo simulation feature of the DFY tool WiCkeD [8]. The original design had an overall yield of 72 % within the allowed temperature range (T= –40°C to T= +85°C) where the yield at the critical operating point (T= –40°C) was 73 % whereas $V_{TRIG,min}$=2.6V and $V_{TRIG,max}$=4.1V (see Fig. 4).

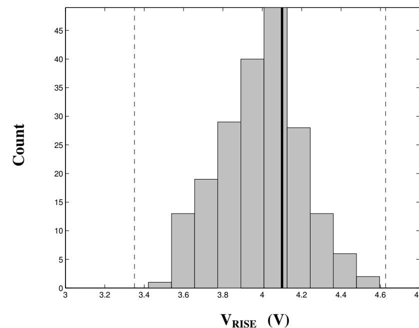

Fig. 4. Monte Carlo simulation: Histogram of the threshold voltage V_{TRIG} for the original design at T= –40°C, Yield=73%. Specification (solid line) and simulated 3σ limits (dashed line).

The Monte Carlo simulation at the critical operating point (T=-40°C) results in the following mean and standard deviation for the output threshold voltage V_{TRIG}: $\mu = 3.98\,V$, $\sigma = 0.212\,V$.

3.2 Sensitivity Computation

The subsequent sensitivity computation provides information concerning the sensitivities with respect to process parameters.

The main contributors concerning the variance of V_{TRIG} are determined by:

- the process variation of the PMOS threshold voltage *delvt_p* (59% relative influence)
- the process variation of the NMOS threshold voltage *delvt_n* (21 % relative influence)
- the process variation of the effective channel width *del_xw* (18 % relative influence).

The biggest influence is given by the variation of the PMOS threshold voltage where the sensitivity with respect to V_{TRIG} has been determined from the Monte Carlo analysis assuming a standard deviation of $\sigma_{VTP} = 30mV$ (see Table I) by:

$$S_{VTP} = \frac{dV_{TRIG}}{delvt_p} = -0.188\,V/\sigma_{VTP} = -0.188V/0.03V = -6.3 \quad (2)$$

$$\Delta V_{TRIG} = S_{VTP} \cdot \Delta VTP \quad (3)$$

This information is used to calculate an appropriate shift of the PMOS threshold voltage in order to increase the yield of the original design during production.

The sensitivity analysis and optimisation features of the DFY tool WiCkeD are based on an analytical model of the circuit behaviour as described in the remainder of this paragraph. Three parameter spaces are distinguished: The design parameters denoted by the vector $\mathbf{d}$ (e.g. drawn lengths and widths of transistors), the operating parameters (e.g. temperature or supply voltage) combined in the vector $\boldsymbol{\theta}$ and the statistical parameters $\mathbf{s}$ describing the global and local process variation (1). The statistical parameters can always be normalized to be Gaussian distributed with mean value $\mathbf{s_0} = \mathbf{0}$ and standard deviation $\boldsymbol{\sigma} = \mathbf{1}$ for each component. As far as the design properties are concerned, the components of the vector $\mathbf{f}(\mathbf{d}, \mathbf{s_0} - \mathbf{s}, \boldsymbol{\theta})$ are the specified performances of the design (the threshold voltage V_{TRIG} in this example) and the specification vector $\mathbf{f_b}$ describes the upper and/or lower bounds for all performances. A circuit meets all specifications if the expression $\mathbf{f}(\mathbf{d}, \mathbf{s_0} - \mathbf{s}, \boldsymbol{\theta}) < \mathbf{f_b}$ holds true. Finally, the yield $Y(\mathbf{d}, \mathbf{s_0})$ is the percentage of manufactured devices which meet all specifications over the whole range of operating conditions and can be expressed as

$$Y(\mathbf{d}, \mathbf{s_0}) = \iint_{\{\mathbf{s} | \mathbf{f}(\mathbf{d}, \mathbf{s_0} - \mathbf{s}, \theta) < \mathbf{f_b} \ \vee \ \theta\}} pdf(\mathbf{s_0} - \mathbf{s}) d\mathbf{s} \qquad (4)$$

Details on the computation of this integral can be found in [6]. Sensitivity analysis is supported both for the performances (deviation of a performance with respect to a parameter) and the yield (deviation of the expression for yield with respect to a design parameter or the mean value of a statistical parameter). In the present investigation sensitivity analysis of the performance with respect to the statistical process parameters has been applied.

4 Yield Enhancement by Shift of Process Parameters

As seen from Fig. 4 the 3σ limit of V_{TRIG} at T=-40°C (4.6 V) is 500 mV too high with respect to the specification (upper limit V_{TRIG} =4.1V). Since the PMOS threshold voltage is the main contributor to the variation of V_{TRIG} an appropriate shift of the typical PMOS transistor threshold to decrease V_{TRIG} by 500 mV can be calculated from the sensitivity S_{VTP} (2) by

$$500 = 6.3 \cdot \Delta VTP \Rightarrow \Delta VTP = 79mV \qquad (5)$$

Therefore, an increase of the nominal threshold voltage by +79mV (VTP=-0.76 shifted to VTP=-0.68V) is able to lower the maximum output by 500 mV and enables a 3σ design for the given operating point. The increase of the yield is verified by Monte Carlo simulation assuming shifted process parameters vtnom=-0.68V in (1) and results in the following mean and standard deviation for the output threshold V_{TRIG}: $\mu = 3.7V, \sigma = 0.21V$ and a simulated overall yield of 98 %. The shift of the nominal threshold voltage has been implemented for the given production process by a corresponding decrease of the PMOS threshold adjust implant dose (implant dose was changed from 3.4e12/cm^2 to 3.5e12/cm^2 with an implant energy of 70keV). The implemented solution led to a yield increase of 15% for the original design during production.

5 Yield Optimisation by Design Centering

For the intended re-design of the power-on reset cell the yield optimization feature of the DFY tool WiCkeD is used. This special program optimizes design parameters for highest yield. The yield optimization is based on the worst case distance in the statistical parameter space. The worst case distance in the statistical parameter space is best explained on the basis of the integration region of expression (4).
The worst-case point $\mathbf{s_{wc}}$ is the set of values of the process parameter vector that is most likely to occur during the manufacturing among all process parameter vectors that make the circuit violate one specification. For a given assignment of the parameter vector $\mathbf{d}$, the worst case point $\mathbf{s_{wc}}^i$ for specification i is defined as:

$$\mathbf{s_{wc}}^{\mathbf{i}}(\mathbf{d}) = \mathrm{argmin}\{(\mathbf{s_0}^{\mathbf{T}} - \mathbf{s}^{\mathbf{T}})(\mathbf{s_0} - \mathbf{s}) \,|\, f^i(\mathbf{d}, \mathbf{s_0} - \mathbf{s}) = f_b^{\,i}\} \qquad (6)$$

The worst-case distance $\|\mathbf{s_{wc}}^i - \mathbf{s_0}\|$ between the worst-case point to the nominal value determines the yield of performance no. *i*.: a large value of $\|\mathbf{s_{wc}}^i - \mathbf{s_0}\|$ indicates a high yield and vice versa. The automatic yield optimization algorithm of WiCkeD estimates yield by worst case points. This enables a calculation of the sensitivity of yield regarding design parameters, which is not possible from a Monte Carlo simulation.
By this yield optimization, a new solution vector **d** was found that resulted in a yield increase of more than 20 % by changing only 3 transistor parameters: the channel lengths of two PMOS load transistors (L4 and L13) and of an NMOS transistor (L7). The values of the transistor parameters cann be seen in Table II. The moderate area increase of the optimized design enables an easy replacement of the original cell without increasing the original layout area reserved for this block. The yield increase was verified performing a Spectre-Monte Carlo simulation within the Cadence [1] design environment (see Fig. 6).

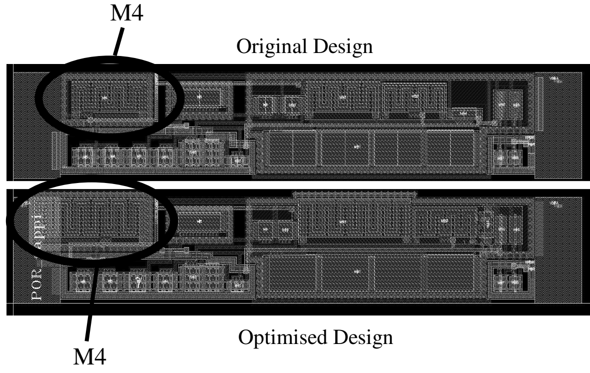

Fig. 5. Layout of the original design (upper) and the optimised design (lower).

The total computation time for the yield optimization was one hour using a parallel LSF-based simulation environment and 5 servers.

TABLE II

Yield optimisation results for power-on reset cell.

	Original Design	Optimised Design
Monte Carlo Simulation at –40°C	Y=73% μ=3.98V σ=212mV	Y= 98% μ=3.7V σ=191mV
Total Yield	Y=72%	Y=93%
Design Parameters	L7=6μm L4=L13=75μm Area=2055μm²	L7=7μm L4=L13=150μm Area=2446μm²

The yield increase was verified performing a Spectre-Monte Carlo simulation within the Cadence [1] design environment (see Fig. 6 and Table III).

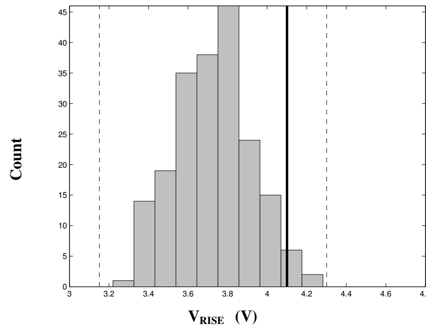

Fig. 6. Monte Carlo simulation: Histogram of the threshold V_{TRIG} for the optimised design at worst-case-operating point T=-40°C, Yield=98%. Specification (solid line) and 3σ limits (dashed line).

6 EXPERIMENTAL RESULTS

For experimental verification the yield of the optimised design is compared to the yield of the original design by production measurements on wafer level (wafer sort). Therefore, a process window verification is used. The wafers of a specific production lot are processed in different ways and a production split reflecting different corner conditions is applied (group 1: typical mean, group 2: worst-case-power, group 3: worst-case-speed, group 4: worst-case-one and group 5: worst-case-zero). The worst-case-conditions for the NMOS and PMOS threshold voltage are spanning a rectangular area over the allowed specification (NMOS: 0.68V to 0.84V and PMOS: -0.68V to -0.88V). The groups are realized by varying the threshold adjust implant dose for NMOS and PMOS transistors. A good yield over all split groups is equivalent to a long-term production stability. For the power-on reset cell the defined process window is especially suitable to verify the robustness since the variation of V_{TRIG} mainly relies on the PMOS threshold variation as determined by the sensitivity analysis. During electrical wafer sort, the threshold voltage V_{TRIG} is monitored at T=35°C and a test limit V_{guard}=3.9 V is implemented in order to screen out bad parts at low temperature (parts with V_{TRIG} > 4.3 V at –40°C). This guard band limit is implemented to avoid a low temperature sort and is calculated from the linear temperature slope of the reset voltage (TK = -5.8 mV/K). The original design had a measured mean value $\mu = 3.73V$ and a standard deviation $\sigma = 0.3V$ for all split groups. The total yield of the original design is 69 % (n= 493 out of 606 parts) and close to the Monte Carlo simulation results (72 %). As expected from the sensitivity analysis the most critical corner for this design is the worst-case-speed corner (large magnitude of PMOS threshold and NMOS threshold voltage). For the original design, all parts are out of specification for the worst-case-speed corner (see Fig. 7).

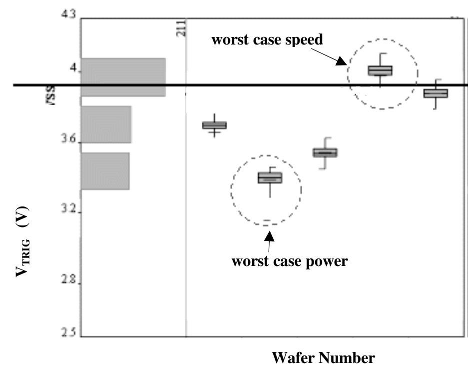

Fig. 7. Original design: Histogram and Box Plots for measured reset voltage and different split groups. Total measured yield is 69 %. Wafer test limit V_{guard}= 3.9V .

As predicted by simulation a clear improvement of production yield can be seen for the optimised design (see Fig. 8) with a measured mean value μ=3.38V and a standard deviation σ=0.23V.

For the optimised design all measured parts lie below the critical production limits (V_{guard} = 3.9V) and the yield is 100%

for all split groups (n=997 parts). The measured worst-case-distance (sigma to target) increased from 0.6σ for the initial design to 2.3σ for the optimised design at the low temperature corner.

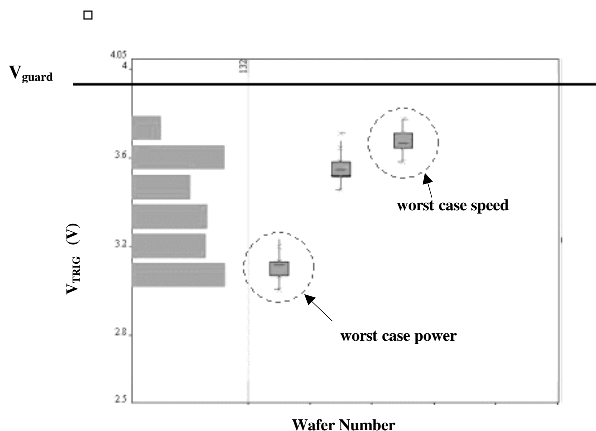

Fig. 8. Optimised design: Histogram and Box Plots for measured reset voltage and different split groups. Total measured yield is 100 %. Wafer test limit V_{guard}= 3.9V .

Figure 9 compares the histogram of the critical worst case speed corner for the original (a) and the optimised design (b). For the original design all parts are above the test limit of 3.9V. For the optimised design all parts are below the test limit with an additional safety margin of 100mV to the guard band.

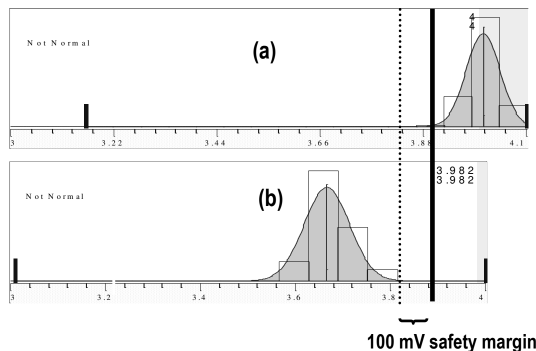

Fig. 9. Worst case speed corner of the original (a) and the optimised design (b). Test Limit = 3.9V (solid line)

7 CONCLUSION

A yield optimisation of an IP block (power-on reset cell) was carried out using automated simulation based design centering and verification by experimental results. First, critical process parameters have been determined by sensitivity analysis allowing the improvement of production yield (15%) for the initial design by adjusting the PMOS threshold implant dose. In a second step a new set of design parameters was determined by simulation based yield optimisation where the goal was to keep the device area as small as possible and to maximize the worst-case-distance. The simulated yield improvement (25%) for the optimised design was experimentally proven by process window verification. The quality of the simulation results heavily relies on the accuracy of SPICE simulation models (Monte Carlo models) reflecting the global and local variations of the production process.

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