

# Circuit Design-for-Yield (DFY) for a 110dB Op-Amp for Automotive and Sensor Applications

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## Abstract

The scope of this paper is to show how tools for analog design automation can assist a modern topology design on the example of a High Gain Operational Transconductance Amplifier (OTA). A design method is presented that involves a combination of topology improvement and yield optimization by utilizing the tools zmdAnalyser and WiCkeD.

We used the possibility to interactively analyze and size the circuit design for an exhaustive analysis of a hierarchical circuit as well as to understand limitations of different circuit topologies. In this way, we achieved a final topology with a high simulated parametric yield.

The OTA is designed for ZMD's 0.6 $\mu$  standard CMOS technology. The design contains about 130 active devices and measures 300x300 $\mu$ m<sup>2</sup>. Taking into account process variation, mismatch, the large automotive temperature range and a supply voltage range of 5V  $\pm$ 10%, a dc gain of more than 110dB and a unity-gain frequency greater than 50MHz for a 9pF load were achieved. The settling time is less than 100ns with an accuracy finer than 0.025%. The consumed supply current is about 2.5mA.

## 1 Introduction

There are many challenges specific to analog design automation: The basic structural elements of design (transistors) behave and interact in a complex manner. The important characteristics of advanced analog circuits are often difficult to approximate as symbolic expressions of design parameters and other influences. Numerical circuit simulators work well and are an established tool used for analog design, but they provide only a limited set of analyses and give little insight into the optimization potential of a circuit. Many analog circuits' specifications have challenging trade-offs and require multi-dimensional, multi-objective optimization. Defining specifications for sub-blocks of the circuit is often not obvious at all, which is an obstacle to top-down design. Operating conditions like temperature, parasitics and process variability like V<sub>th</sub> mismatch are often critical for a circuit's performance, but these effects unfortunately depend on the chosen circuit topology, specification and sizing. Simple corner simulation often fails to give a realistic view of the manufacturability of an analog design. In practice, structural design of the circuit topology is not clearly separated from tuning design parameters. Both tasks are performed together, based on numerical simulation results and the designer's experience and intuition.

Despite their importance, design automation for analog circuits still lags behind that of digital circuits, and it is widely accepted that both quality and design time of current analog designs could benefit from supporting analog designers with more advanced methods and tools for analysis and optimization of their designs.

In this paper, we show for a rather difficult analog design, the tools zmdAnalyser [1] and the tool set WiCkeD [2], how such methods can be efficiently integrated into the analog design work and which advantages can be gained.

In section 2, the design problem is introduced. Section 3 gives an overview and references on the background of the applied methods for analog design automation. Section 4 then shows the actual design steps that were performed and the results. [1]

## 2 High DC Gain Amplifier

### 2.1 Specification and Design Goals

The amplifier is the most critical analog block within the design of a 14 bit *cyclic redundant signed digit* (RSD) ADC. It is critical for the high accuracy of this ADC, that a certain internal analog multiplication is performed with very high accuracy, which in turn depends on the dc gain of the OTA cell of Figure 1.

In detail a dc gain better than 110dB is demanded [3]. Another challenge is the settling time, which has to be faster than 100ns for a capacitive load of 3pF–9pF.

The trade off between high dc gain and settling time could not be solved by available topologies. In literature, solutions for smaller temperature ranges were published [4]. But the wide temperature range from –40° C up to 150° C which is typical for automotive applications, makes the design task very difficult and requires a new design.

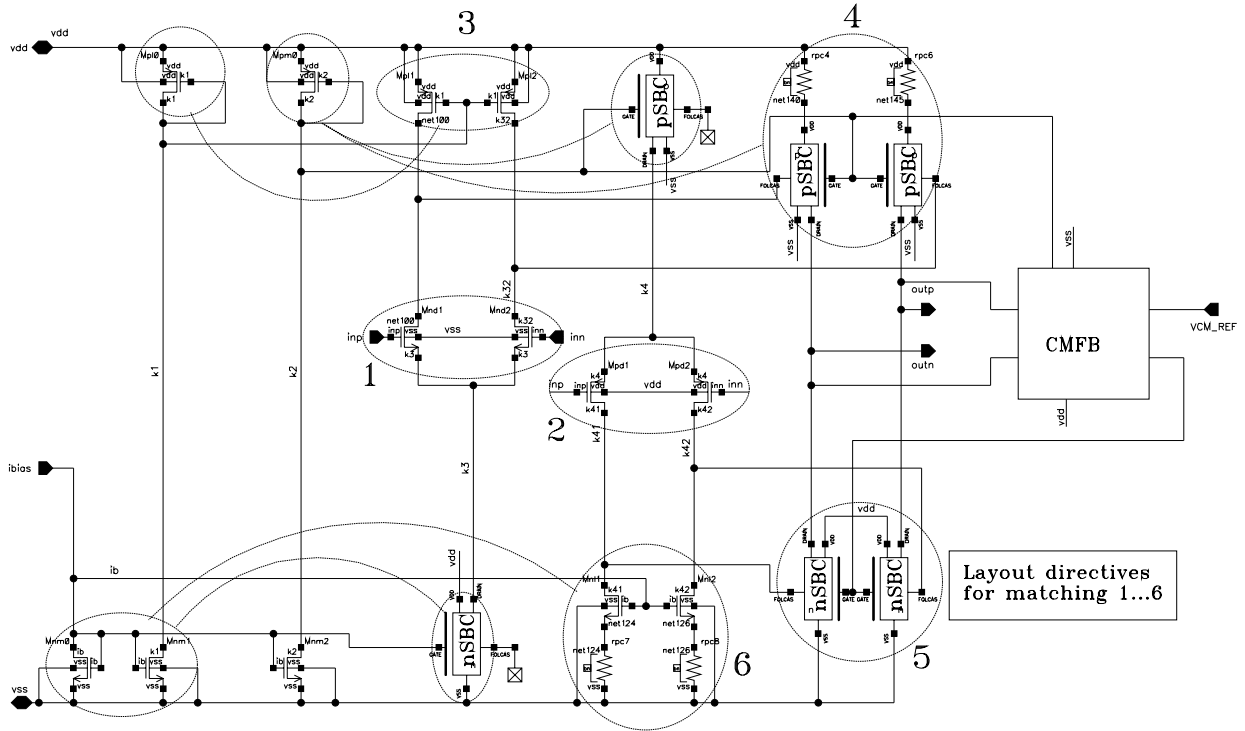


Figure 1: Simplified schematic of the fully differential folded cascode OTA.

## 2.2 New folded cascode circuitry

Fig. 1 shows the simplified circuit of the final realization. As a basic principle, we replaced simple cascodes of a common OTA structure by SBC. Based on earlier design analyses, we adapted cascode structures with gain boosting effect [5, 6] to realize the demanded high dc gain. Such enhanced cascode structures are also known as regulated cascodes or better *self biasing cascodes* (SBC). The SBC circuits (denoted “pSBC” and “nSBC” in Figure 1) consist of 12 transistors each. The purpose of these blocks is to show a characteristic similar to a single transistor but with a much higher output resistance of up to a few 100M $\Omega$ . When we started the design of the circuit, it was unclear if all cascodes of the structure have to be implemented as SBC in order to achieve the high gain, or if some can be kept unchanged. Furthermore, it was unclear whether all SBC structures could be sized equally which would simplify the layout, or if it is necessary to consider different sizings for SBC in different stages of the circuit.

Additionally, we chose complementary folded cascode techniques for the new OTA design [7]. Not shown in Fig. 1, we introduced clamp circuitry for speed and stability purposes, see [8].

Utilizing SBC, the new OTA circuitry showed promising first simulation results at nominal conditions especially for the high dc gain. But achieving a high robustness of gain and settling time over process variation and operating range was a challenge. The initial structure was quite complex and contained 190 devices. Many of them could be sized independently, which resulted in more than 100 degrees of freedom for sizing. This high complexity together with the sensitivity to technology and operating conditions demanded a

step by step design improvement that heavily relies both on automatic optimization techniques and on the designer’s experience.

## 3 Methodology

### 3.1 Structural Constraints

Analog circuits are composed of basic building blocks like current mirrors or differential pairs. Unlike digital gates, the analog ones depend on their geometries and operating point to operate correctly. Usually, being in saturation is an important constraint on many analog transistors, as well as current symmetries or certain nodes being at the same potential. Since these constraints are neither related to the specification, nor to the layout level like design rules are, but come from the structure of the circuit, they are called “structural constraints”. We distinguish four types of constraints:

1. geometric equality, like “equal lengths  $l_1 = l_2$  in a current mirror”
2. geometric inequality, like “ $w_1 l_1 > 6L_{\min}^2$ ”
3. electrical equality, like “ $I_1 = I_2$ ” in a current mirror
4. electrical inequality, like “ $V_{gs} - V_{th} > 50\text{mV}$ ” (strong inversion)

The geometric constraints can be guaranteed by construction. To check the electrical inequality constraints, a simulation has to be done that shows by which amount  $c_k$  each constraint  $k$  is overfulfilled ( $c_k > 0$ ) or is violated ( $c_k < 0$ ).

Like design rules on layout level, structural constraints on schematic level do not at all guarantee that the circuit fulfills

the specification, but a violation indicates a structural problem that may result in a low yield but remains undetected when simulating a rather high-level circuit specification.

For a typical analog circuit consisting of 100 transistors, more than 400 constraints may be created. Since many structural constraints can be derived from requirements on basic structures like current mirrors, generation of many of these constraints can be performed automatically [9].

### 3.2 Feasibility Optimization (FO)

Structural constraints are useful to automatically find a good initial sizing and to ensure that tools for automatic nominal optimization and design centering provide technically feasible results [10]. For that purpose, FO modifies the vector  $\mathbf{d} = (d_1, \dots, d_{n_d})$  of design parameters (like transistor geometries and resistor values) so that all constraints are fulfilled, i.e.,  $\mathbf{c}(\mathbf{d}) \geq \mathbf{0}$ . Usually, a reasonable initial sizing  $\mathbf{d}_{\text{init}}$  is available and a solution close to it is preferred:

$$\begin{aligned} \min_{\mathbf{d}} \|\mathbf{d} - \mathbf{d}_{\text{init}}\| \\ \mathbf{c}(\mathbf{d}) \geq \mathbf{0}. \end{aligned} \quad (1)$$

The number of independent design parameters  $n_d$  grows with the number of elements to be sized and is reduced by geometric equality constraints. For a typical analog circuit consisting of 100 transistors,  $n_d$  can be expected to be between 15 and 30, with complex designs like the presented OTA having up to 100 degrees of freedom.

### 3.3 Nominal Optimization (NO)

Analog circuits are characterized by performance measures, for example, gain  $A_0$ , slew rate SR, noise figure NF. The specification requires the values of these measures not to exceed certain upper and/or lower bounds, for example  $A_0 \geq 80$  dB.

We denote the performance measures by the vector  $\mathbf{f} = (f_1, \dots, f_{n_f})$ , with the vectors of lower bounds  $\mathbf{f}^L$  and upper bounds  $\mathbf{f}^U$ . The performance measures depend on design parameters:  $\mathbf{f}(\mathbf{d})$ , and the specification is

$$\mathbf{c}(\mathbf{d}) \geq \mathbf{0} \quad \wedge \quad \mathbf{f}^L \leq \mathbf{f}(\mathbf{d}) \leq \mathbf{f}^U. \quad (2)$$

The goal of nominal optimization is finding values for  $\mathbf{d}$  that satisfy (2).

Moreover, this must be achieved for a defined range of operating parameters like temperature or Vdd. We denote the operating parameters by the vector  $\boldsymbol{\theta} = (\theta_1, \dots, \theta_{n_\theta})$ . Then,  $\mathbf{f}$  depends also on the operating conditions:  $\mathbf{f}(\mathbf{d}, \boldsymbol{\theta})$ , and the specification is

$$\mathbf{c}(\mathbf{d}) \geq \mathbf{0} \quad \wedge \quad \forall_{\boldsymbol{\theta}^L \leq \boldsymbol{\theta} \leq \boldsymbol{\theta}^U} \mathbf{f}^L \leq \mathbf{f}(\mathbf{d}, \boldsymbol{\theta}) \leq \mathbf{f}^U. \quad (3)$$

The goal of nominal optimization with operating conditions is finding values for  $\mathbf{d}$  that satisfy (3).

Two types of algorithms are available for nominal optimization in WiCkED: gradient-based optimization with parameter distances [11] and stochastic (global) optimization.

The nature of most analog sizing problems is optimization of performance functions that show strong tradeoffs, are expensive to evaluate in terms of simulation time, but are monotonous or convex—not in the full design space but in the small feasible design space that is restricted by the large number of structural inequality constraints. Gradient-based methods can be adapted to this type of problem very efficiently. Therefore it is reasonable to run these methods first, and to resort to stochastic optimizers only when simulation results and design knowledge indicate that multiple local optima actually exist.

### 3.4 Design Centering (WCA, YO)

Process variation and mismatch have a large influence on the performance measures of analog circuits. For simulation, this effect is modeled by varying randomly a few standard normally distributed model parameters, for example  $\text{tox}$  or  $V_{\text{th}}$ . The vector of random model parameters is denoted by  $\mathbf{s} = (s_1, \dots, s_{n_s})$  with mean value vector  $\mathbf{0}$  and unity covariance matrix. Process variation and mismatch are both contained in  $\mathbf{s}$ , so for a typical analog circuit consisting of 100 transistors,  $n_s$  can be expected to be between 200 and 250.

One standard method for estimating the distributions of performance measures is Monte Carlo simulation. A sample of size  $N$  of  $\mathbf{s}$  is generated and simulated, yielding  $N$  result vectors  $\mathbf{f}^{(i)} = \mathbf{f}(\mathbf{d}, \boldsymbol{\theta}, \mathbf{s}^{(i)})$ ,  $i = 1 \dots N$ . The parametric yield  $Y$  is estimated as the percentage of samples that lie within the specification bounds ( $\mathbf{f}^L, \mathbf{f}^U$ ). Monte Carlo is only an analysis method, but does not vary  $\mathbf{d}$  and hence shows little information on how to improve the yield by changing  $\mathbf{d}$ .

Yield improvement can be accomplished by worst-case distance methods. A design that satisfies (3), i.e., that fulfills the specification for the typical process and no mismatch ( $\mathbf{s} = \mathbf{0}$ ) and for all required operating conditions, could still violate the specification for some  $\mathbf{s} \neq \mathbf{0}$ . If process conditions  $\mathbf{s}$  causing violations are close to the mean value (i.e.,  $f_i(\mathbf{d}, \boldsymbol{\theta}, \mathbf{s}) < f_i^L$  for some  $\boldsymbol{\theta}$  and small  $\|\mathbf{s}\|$ ), then there will be severe parametric yield loss. Therefore, an important measure for a performance  $f_i$  is the worst-case distance  $\beta_{\text{wc}}^{(i)}$ , which is the shortest distance between the mean value and a process condition that causes  $f_i(\mathbf{d}, \boldsymbol{\theta}, \mathbf{s})$  to fail its specification. For a lower bound  $f_i^L$  of a spec that satisfies (3),

$$\begin{aligned} \beta_{\text{wc}}^{(i)} &= \min_{\boldsymbol{\theta}, \mathbf{s}} |\beta| \\ f_i(\mathbf{d}, \boldsymbol{\theta}, \beta \frac{\mathbf{s}}{\|\mathbf{s}\|}) &= f_i^L \\ \boldsymbol{\theta}^L \leq \boldsymbol{\theta} \leq \boldsymbol{\theta}^U. \end{aligned} \quad (4)$$

The worst-case distance for an upper bound is similarly defined.

A worst-case distance is a function of the design parameters. They are useful goals to maximize over  $\mathbf{d}$  and thereby achieve a design that is centered in the process space regarding the specification bounds [12, 13].

## 4 Flow and Results

The design was performed in five main design steps A–E (see Tab. 2). Every step was supported by the analysis and optimization flow of WiCkeD. In this way, we discovered topology limits at different design steps and were able to enhance the topology. Step by step, our understanding of the circuit problems improved, too.

**A: Feasibility of main topology.** A first implementation of the new topology with all cascodes implemented by SBC was drawn together with a suitable testbench. Feasibility optimization (FO) showed that it is quite difficult but possible to satisfy all saturation constraints inside the SBCs. A couple of nominal optimization (NO) runs on variations of the topology and in reduced parameter spaces showed that the high gain specification can also be achieved with fewer cascodes replaced by SBC, and that most SBCs can be sized identically.

**B: Optimization of the SBC sub-blocks.** As a hierarchical approach to the design of this circuit, we took the SBC sub-blocks from the Op-Amp and tried to optimize them individually. Deriving a specification for the SBCs from the specification of the Op-Amp in a top-down manner turned out to be very difficult. Secondly, analog sub-blocks like the SBCs cannot be simply cut out of their environment, because the rest of the circuit interacts with them and must be considered during simulation.

Although the top-down design experiment did not succeed, separately constraining and optimizing the SBC blocks created important insights into their sensitivities. We found an essential saturation constraint that guarantees a high output resistance of the SBCs. Furthermore, we identified sensitivities to parasitics at certain nodes inside the SBCs. Hence we were able to calculate the maximally acceptable values of these parasitics before the SBC fails to operate. This information is valuable for layout verification.

**C: Optimization of main circuit.** After including the additional SBC saturation constraint and replacing an idealized model of the CMFB with a real circuit (see [14]), the feasibility optimization was completed successfully by WiCkeD. The performance parameters of the amplifier could be improved significantly by nominal optimization. Unfortunately the circuit became unstable because the loop consisting of the *common-mode feedback* (CMFB) circuit and the OTA became unstable. As a consequence, the phase margin of this loop had to be included as a design constraint  $\phi_m > 25^\circ$ . We extended the test bench to calculate this phase margin by means of a loop gain simulation. A new run of the nominal optimization then resulted in a stable circuit.

**D: Yield analysis and optimization.** We applied Monte Carlo analysis to estimate the variation and parametric yield of the performances. It turned out that most specifications of the design were in the higher 95% range of yield, but about

30% of the sample failed the settling time or the phase margin of the CMFB loop.

In order to improve the stability of the CMFB loop further, we introduced an RC lowpass at an internal node of the CMFB structure.

The analysis of the effects of process variation, mismatch and operating range pointed out critical design parameters, so that we could reduce the parameter space: For optimization of the robustness of settling time, we kept constant most of the design parameters of the SBC and focused on the clamp circuit and on the differential input stage that we knew to be the part that has the most influence on settling time.

**E: Final centering, rounding and verification.** We applied design centering by worst-case distances including operating conditions. Finally, the design parameters were adjusted to the technology grid, and the result was checked again by worst case analysis (WCA) and Monte Carlo analysis (MC). The results are shown in Tab. 1 and the layout in Fig. 2. The worst case distance of the parameters are well balanced and predict a high yield.

Performance	Value	Comment
DC Gain	>110dB	
GBW	>50MHz	
Settling time	<100ns	error < 0.025%
Area	300x300 $\mu\text{m}^2$	0.6 $\mu$ CMOS
Supply current	$\approx$ 2.5mA	@ 5V
Yield prediction	$\approx$ 98%	

Table 1: Performances of the OTA with key parameters. Operating range: temp:  $-40^\circ\text{C}$  up to  $150^\circ\text{C}$ , capacitive load: 3pF up to 9pF, power supply:  $5 \pm 0.5\text{V}$ .

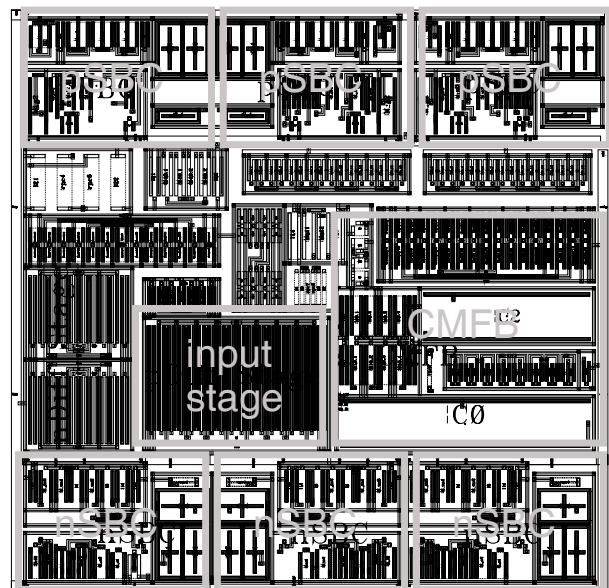


Figure 2: Core layout of the realized OTA.

Step	WiCkeD modules	Testbench	used sizing parameters count		
			main	SBC	CMFB
A	FO, NO	diff. OTA	20 of 20	4 x 20 of 20	ideal
B	FO, NO, MC	SBC	—	2 x 15 of 20	—
C	FO, NO, WCO	diff. OTA	4 of 20	2 x 3 of 20	10 of 10
D	MC, WCD, MM, YO	diff. OTA + CMFB stability	10 of 20	2 x 2 of 20	13 of 13
E	YO, WCD, MC	diff. OTA + CMFB stability	4 of 20	—	—

Table 2: Main design steps with used testbench and WiCkeD modules.

Legend: FO Feasibility Optimization, NO Deterministic Nominal Optimization, WCO Worst Case Operation Analysis, MC Monte Carlo Analysis, WCA Worst Case Analysis, WCD Worst Case Diagnosis, MM Mismatch Analysis, YO Yield Optimization.

## 5 Conclusion

We presented a design method utilizing yield optimization techniques to develop a complementary folded cascode OTA with high dc gain. As necessary for analog design, topology modification has to be accompanied by circuit analysis and sizing optimization.

First, the inhouse tool zmdAnalyser and modules of the tool WiCkeD were used for circuit analysis. This resulted in valuable insights into the limitations and trade offs of a new topology. Then, step-by-step design optimization with WiCkeD together with topology modification led to a design that satisfies the specification for a wide range of operating conditions with high yield.

We showed how simplification and extension of the topology together with analysis and optimization techniques helps to better understand the circuitry and to choose an effective design solution. We consider it as important for tools for analysis and sizing of analog circuits to support a fast, interactive and incremental design work flow.

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