

Reuse of Circuit Topologies using WiCkeD

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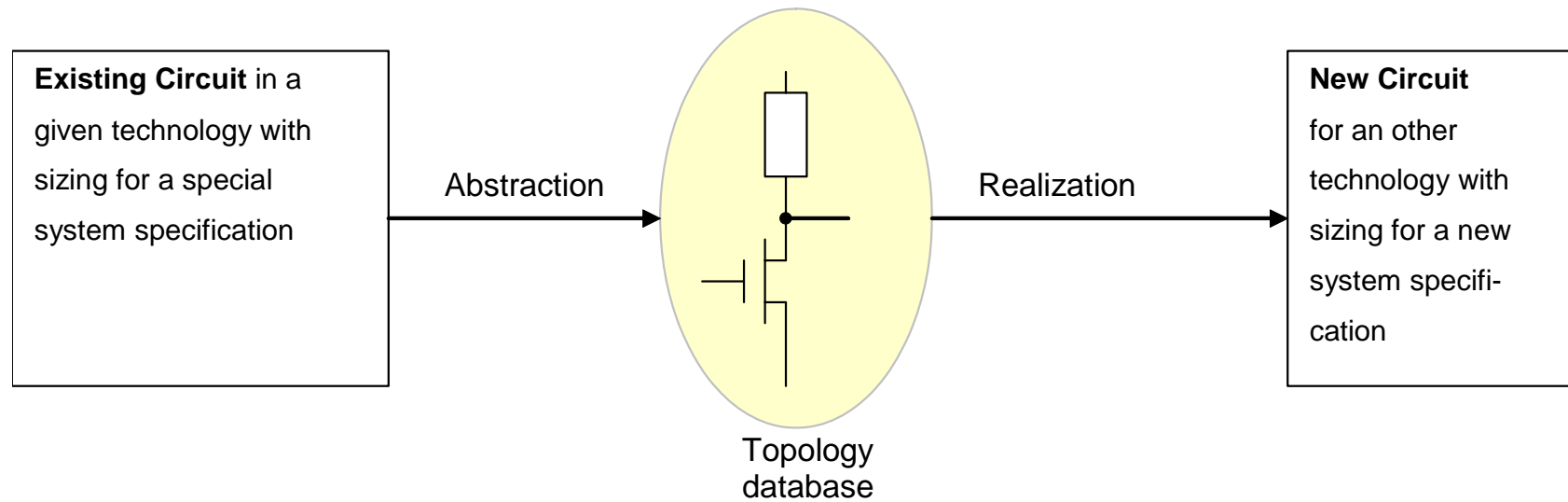
Institut für Mikroelektronik- und Mechatronik - Systeme gGmbH

<http://www.imms.de>

Introduction

- **Design of analog blocks is very time consuming**
- **Automatic synthesis for special cases only**
- **With given topology much easier**
- **Collecting proved and tested topologies in a data base**
- **Process independent storage**
- **Simply to use**
- **Optimizing the topology using WiCkeD**
 - for a process
 - for a specification

Principle of Re-use



Foundations

- **BMBF funding project ANASTASIA2 (2003-2004)**
 - Analysis, modeling and optimizing of analog circuits
 - Tools
 - Symbolic analysis: **AnalogInsydes**
 - Optimizing (sizing, design centering) : **WiCkeD**
- **Funding projekt of ministry of economics in Thuringia „Grundlagen einer Schaltungstopologiedatenbasis für Analogschaltungen“ 2005**
- **Cooperation agreement for WiCkeD between IMMS and MunEDA**

Realization

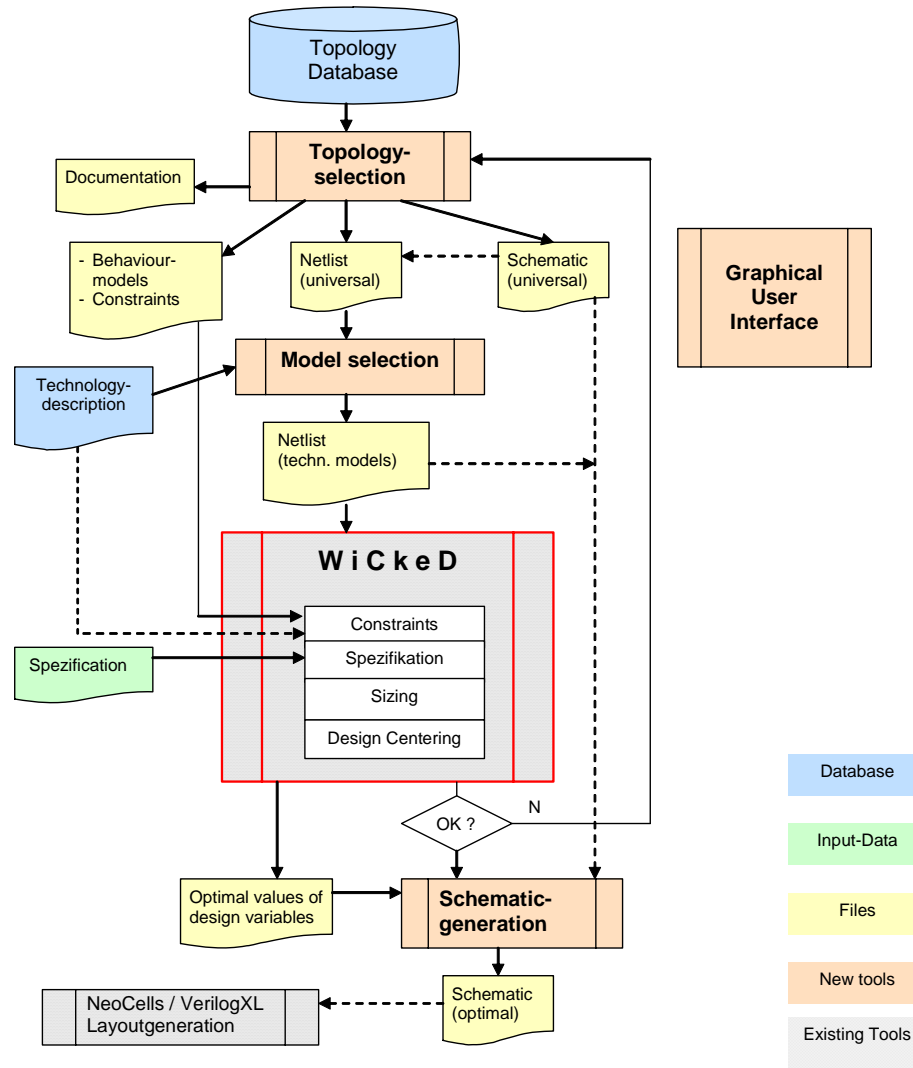
from process independent topology to sized circuit

- **Replace abstract models with process specific models**
 - Simulation with scripts and testbenches
- **Initial sizing**
 - Use of constraints for DC conditions
 - Good starting solution for optimizing
- **Sizing**
 - Nominal optimizing
 - Consideration of environment parameters
- **Design centring**
 - Monte-Carlo Analysis
 - Worst Case Distance Analysis
 - Yield-Optimization
- **Layout estimation**

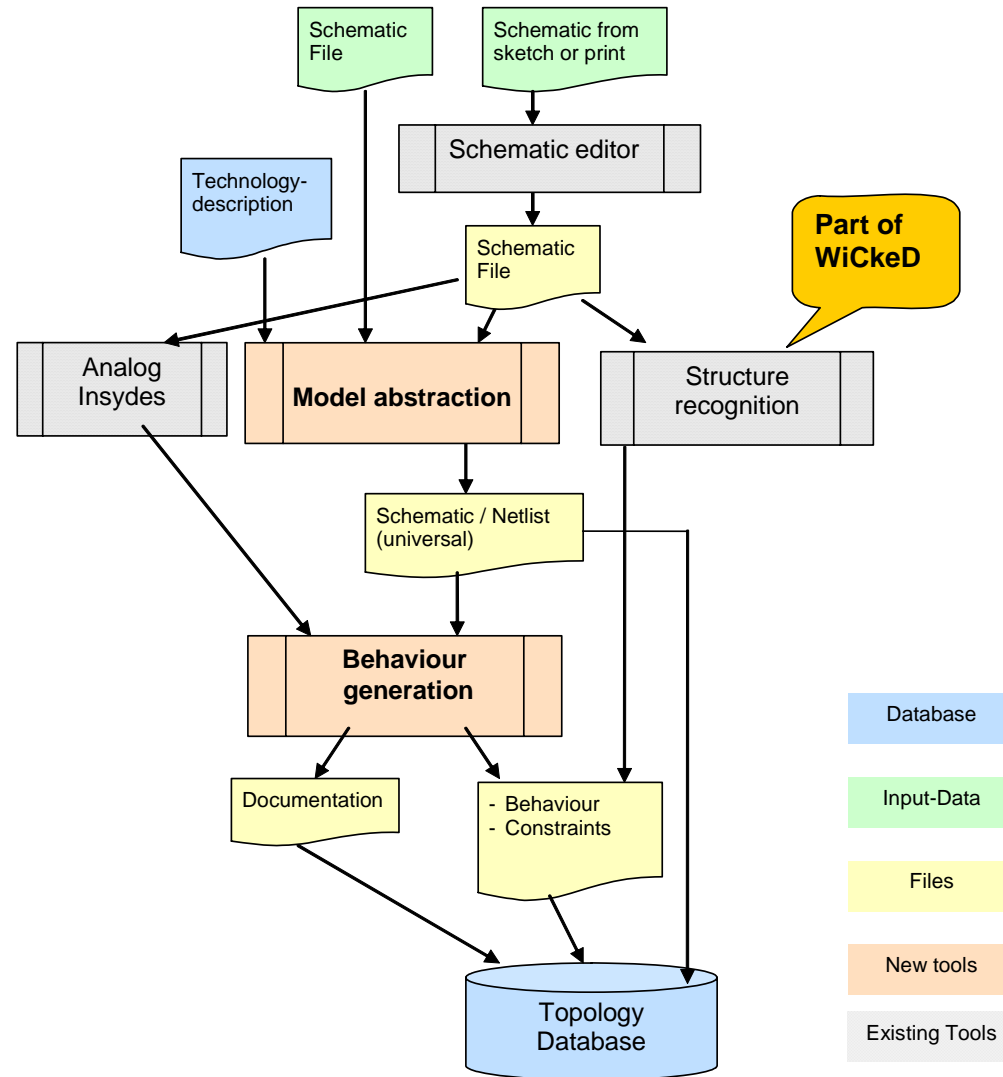


WiCkeD

Realization Overview



Abstraction



Database

- **Topology**
 - Internal link to design data
 - fix preview
 - dynamic generated pixel- and vector graphic
- **Keywords**
 - for searching
- **Description**
- **Constraints**
 - Preliminaries for a working circuit (e.g. DC op point conditions)
- **Testbenches**
- **Simulation scripts**

Technology description

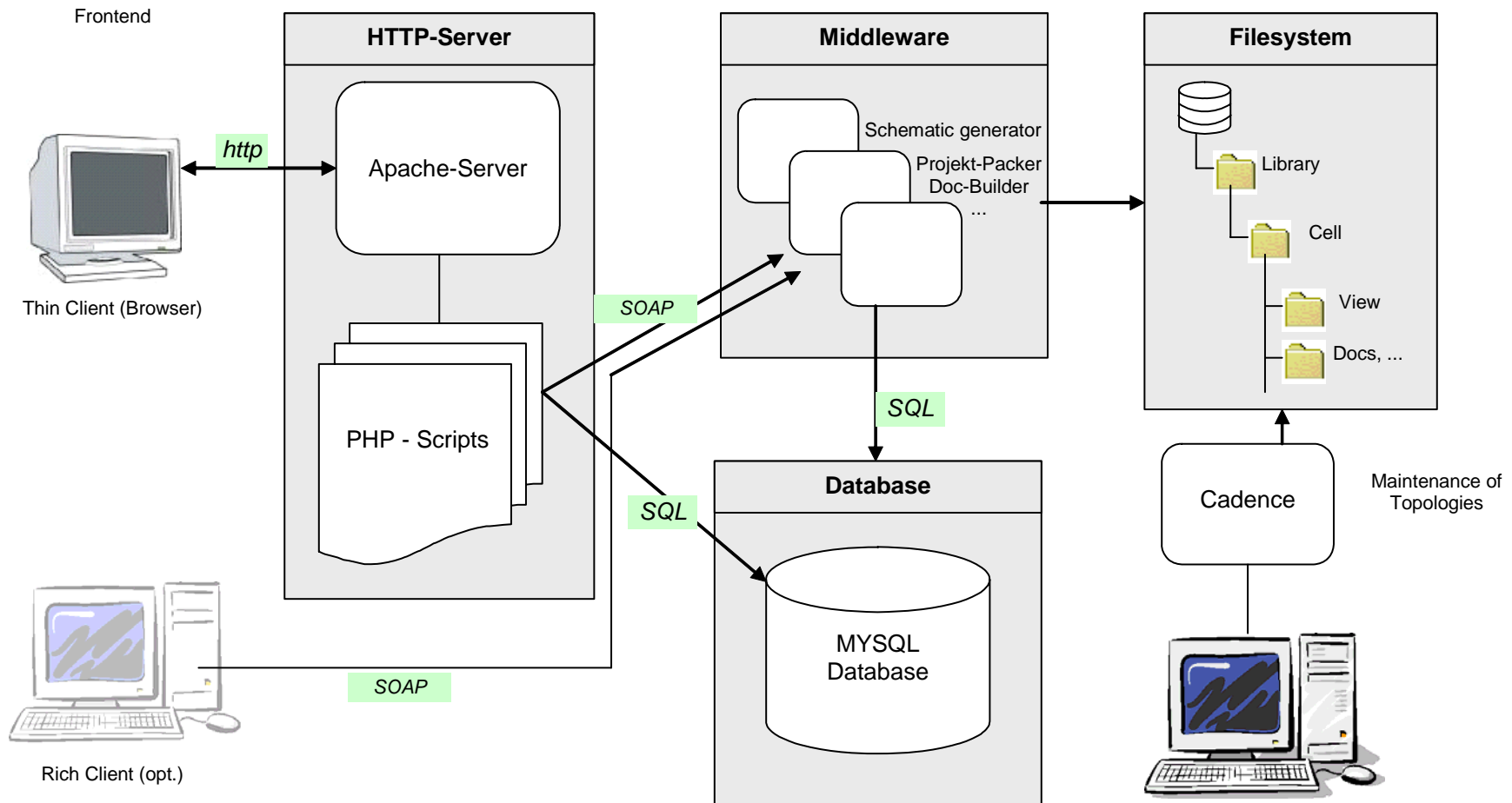
- **For every target process must exist a description for**
 - replacement of abstract device models with appropriate process dependent models
 - recognition of structures to generate constraints
- **This Description must contain:**
 - basic properties (CMOS, BiCMOS, ...)
 - availability of devices (e.g. no pnp for amplifier)
 - assignment of process devices to abstract devices
 - Parameters of device models, parameter bounds
 - technological parameters like power supply voltage, threshold voltage, and others
 - wells

Software Architecture

- **Avoiding installation of software**
- **HTML-GUI for browser**
- **Logic and database on server**
- **Dynamic generation of HTML pages with PHP**
- **Download of projects**
- **Simulation and optimization on client-site**

- **System maintenance tools**

Software Architecture



Graphical User Interface (1)

The screenshot shows a web browser window titled "IMMS Topology Database - Mozilla Firefox" with the address bar displaying "http://apz2.imms.de/". The page layout includes a left sidebar with navigation options, a main header with the IMMS logo and a circuit diagram, and a central content area with a search bar and news section.

Options

Your Login
You must login

Filter
All Topics
Filter

ADC
UpDownCounter_ADC
SAR_ADC
FLASH_ADC
SigmaDelta_ADC

DAC

BIAS CELLS
OTC_bias_cells
PTAT_bias_cells
VBE_bias_cells
Bandgaps
Voltage_Sources
Current_Sources
Gainboosted_Curr_Sources
Current_Limiter
Temperature_Sensors

COMPARATORS

DC SUPPLY
Low_Drop_Out_references
Voltage_regulators
Low_Drop_Out_regulators

DC SUPPLY SWITCHED
Step_Down_Regulators
Buck_Regulators

ESD ANALOG
Analog_Inputs
Analog_Outputs

IMMS Topology Database

Welcome to IMMS topology database.
Here you will find a lot of schematics of analog circuits.

Enter one or more keywords for quick search:
 Search

Here are the latest news.
It will be updated every day.

Topo News

2005-11-15 13:28:17 | vboos | topo online
Topo Database is online now !!!

2005-11-17 11:51:18 | vboos | php works
The start page changed to index.php. So the latest news are visible on start.

Gefördert durch:
 FREISTAAT THÜRINGEN
MINISTERIUM FÜR WIRTSCHAFT, TECHNOLOGIE UND ARBEIT

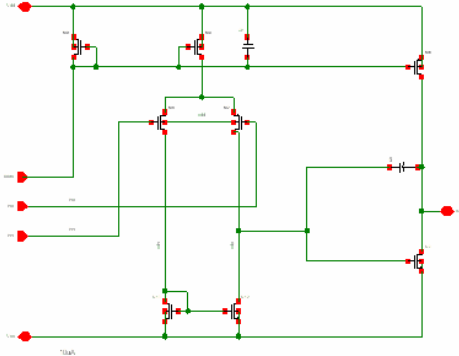
last updated 16 Nov 2005
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Fertig

Graphical User Interface (2)

The screenshot shows a web browser window displaying the IMMS Topology Database. The browser's address bar shows the URL `http://apz2.imms.de/topology.php?id=1&cat=1`. The page title is "IMMS Topology Database" and the breadcrumb trail is "Home > OPAMP > VV_OpAmps". The main content area is titled "Miller OpAmp 2 stage".

Short Description
Miller opamp with p-mos differential input stage and n-mos output stage

Schematic Preview


Keywords
opamp, 2stage, diff, single-ended

Downloads
[Full Description \(.pdf\)](#)
[Project](#)

right side for additional informations

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FLASH_ADC
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DAC

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Analog_Inputs
Analog_Outputs

FEEDBACK NETWORKS

Fertig

Results

Software

- Concept of the architecture
- feasibility studies
- Installation of Apache-Web-Server and MySQL Database
- PHP-Scripts for the most important HTML pages
- Database structure and test data
- Test programs for the middleware

Circuit design

- CADENCE Design-Environment with abstract models
- Testbenches
- Simulation scripts
- Researches for layout estimations

Further Activities

- **Further R&E works necessary**
- **Collaboration in funded projects**
- **Cooperation with MunEDA**
- **Acquire industrial partners**
- **Make possible the use for external partners**