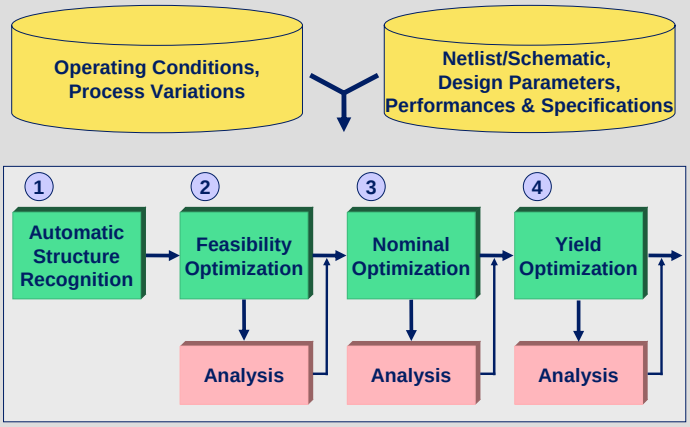
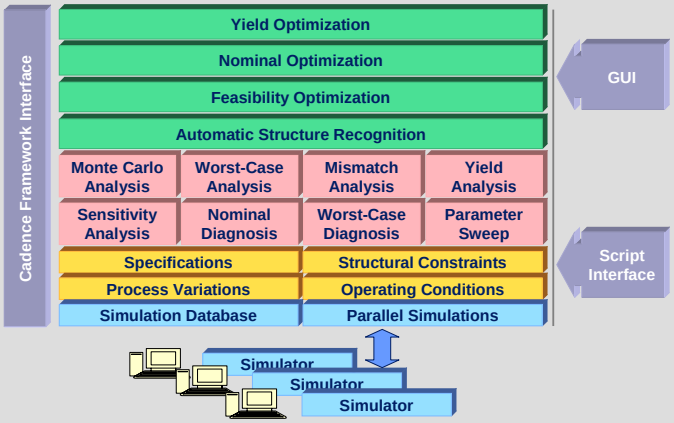
# Analysis and Optimization of Mismatch in Analog Designs

## Yield Optimization of Analog Circuits with WiCkeD

### Design Flow:

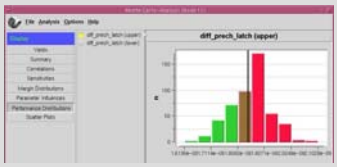



### WiCkeD Features:

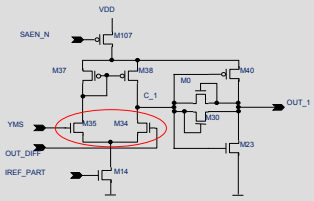



### Example 1

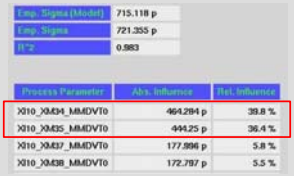
Analysis and optimization of a sense amplifier in 130nm technology. The analysis should especially show the influence of mismatch and temperature.



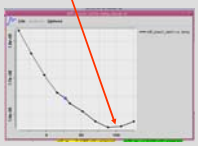
1 **Initial yield analysis showed approx. 40% of yield**
Often the initial sizing fulfils just the performances at nominal conditions, but
•The design should work at all operating conditions
•The sizing of a design for the full range of operating conditions costs a lot of time.




2 **Parameter influence analysis**
Shows the influence of parameters on the yield.
**Result :** ***Two of the parameters have together more than 78% influence. These are mismatch parameters of the transistors M34 and M35.***




3 **Worst case operation analysis**
- Performances have different worst case operating conditions
- WiCkeD calculates the worst case operating conditions for every performance and uses them, even if they are between the 'usual' corners.

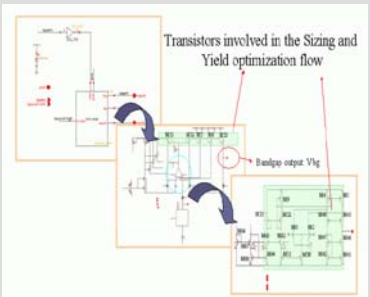


4 **Nominal optimization (not shown)**
Automatic optimization considering local and global process variations. Also operating conditions can be considered.

5 **Worst case analysis**
Calculates the worst case distance (in σ) and determines the yield for every specification under worst case conditions.
**Result:** ***Even before yield optimization the yield is already > 91%. After yield optimization the yield increased to > 98%.***

### Example 2

*(Presented by Carlo Roma at ISQED'05)*
CMOS bandgap for mobile applications, that showed sometimes irregular behaviour on silicon.
**Status:** ***Lack of robustness, best yield was 48%***




1 **Parametrization** is done in the schematic. For a check the Worst Case Analysis is started (see upper region of the right picture).

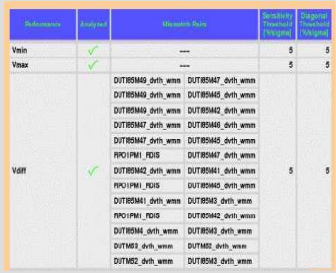
2 **Feasibility optimization (not shown)**
Functional constraints are fulfilled after the optimization.

3 **Nominal optimization**
Optimization of Vdiff, Vmin, Vmax, etc. with all constraints remaining fulfilled. Also the individual worst case conditions of every specification are applied.
**Result:** ***Specifications are now fulfilled for nominal process and operating conditions. The total yield is around 70%.***

4 **Mismatch analysis**
This analysis shows the mismatch pairs with influence on the specifications (see picture).

5 **Yield optimization**
WiCkeD automatically determines the worst-case operating and process conditions for each performance and optimizes the yield.
**Result:** ***Parametric yield is now above 81%!***

6 **Topology change**
The new topology resulted in a ***total parametric yield above 93%!***


**Customer statement**
*This analysis has been useful to demonstrate that the yield loss for the first topology was due to mismatch components, due to the need to generate constant differences and ratios of currents with transistor pairs. The yield has been increased reducing the relevant mismatch pairs after design centering with WiCkeD.*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