

Linear Regulators for High Temperature Applications

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1. Abstract

A linear regulator is one of the building block which is used in almost every electronic system. For high temperatures, the main difficulty is to have a stable reference voltage for different voltage levels. We have investigated two different regulator structures in partially depleted SOI technology with a large temperature range and high power supply rejection. They can be used as voltage references, linear regulators or sub-regulators. One structure is a completely new topology. These structures were optimized with design centering software **WiCkeD**. The methodology for the design centering will be given during the presentation.

2. Regulator topologies

The first topology shown in Fig. 1 was suggested by Ivanov [1]. It is a low drop out voltage regulator. The operation is as follows: If the output voltage decreases because of a decrease of the load resistance, V_{GS} of M_1 decreases. This causes a drop of the potential ϕ_1 . The voltage of source V_2 is comparable to $2V_{TH}$ of the transistors M_2 and M_3 . Therefore $V_{GS,M2}$ increases and M_2 becomes more low ohmic. This causes a drop of the potential ϕ_2 and in that way an increase of $V_{SG,M4}$ and an increase of $I_{D,M4}$, which compensates the decrease of the output voltage. One advantage of the structure is its push pull (Class AB) operation by M_4 and M_3 which improves the PSRR significantly. The quiescent current through M_3 can be controlled by the voltage source V_2 . The implementation of the voltage source can be found at Huisung [2]. Fig. 3 shows the PSRR for different temperatures and the operation with M_3 . All current and voltage sources were replaced by real current and voltage sources and V_1 by a bandgap voltage references. The second topology shown in Fig. 2 is suited for high voltages and in cases where higher drop out are feasible. It is a completely new structure based on the first topology, but M_4 is now a n-channel high voltage MOSFET. This allows much higher operation voltages V_{PS} in our technology, since the p-channel high voltage MOSFETs are limited by the threshold voltage from the backside ($V_{TH,backside} = 25V$). The operation of the structure is very similar to topology in Fig 1a), but the current source I_2 is relaxed by a large resistor R . From Fig 4 one can observe a similar good results for the PSRR. Both regulator structures need a start up circuit to work properly.

3. Optimization of the regulators

Topology Fig. 1 were used for a linear LDO regulator (8V to 5V conversion) which followed a step down regulator (42V to 8V conversion). The whole regulator realizes a high efficiency 5 V regulator for 42V battery powered systems. Within the step down regulator one has to supply the low voltage part with 5.5V supply voltage. This is done with regulators of the second topology (Fig. 2). The step down regulator operates with a switching frequency of 100kHz. So the topologies should have the best possible PSRR at this frequency. They should be immune against spikes and pulse type voltage ripples at the supply lines. The optimization of the regulators are done by design centering tool **WiCkeD**. One has to implement all important transistor, resistor and capacitor sizes as parameters. Then the optimization goals are defined. These are in our case PSRR and step response. Then a sensitivity analysis is done. Here one gets insight which parameters influence the goals e.g. PSRR. The next step is the nominal optimization. All parameters of the parameter sets will be optimized, to achieve the goal parameters. The last step is the real design centering. It contains the deterministic mismatch analysis, worst case analysis and yield optimization. Our optimization strategy for the circuits is as follows. First all subcircuits e.g. V_1 , OpAmp, biasing currents are optimized. Then the whole circuit is optimized for different load conditions. The OpAmp should be fast enough to give no limitation to the PSRR ($f_t > 10MHz$) and should have a high slew rate. The circuits shown in Fig. 1 and Fig. 2 require a bandgap reference V_1 . This bandgap reference has to have a sub-regulator like in Fig. 2 to achieve high PSRR values. After the optimization one can observe the fast step response at the V_{OUT} pin. Further details how to design a high temperature bandgap voltage reference is given at the workshop. Detailed information of the optimization is given at the workshop.

4. Results

Fig 3, Fig 4 show the simulated PSRR of both topologies at different temperatures. Fig 5 and Fig 6. display the high temperature behaviour and the startup and the step response of the topologies. Measurements and results of the optimization for temperature from -40°C to 200°C for both types for voltage regulators will

be presented at the workshop.

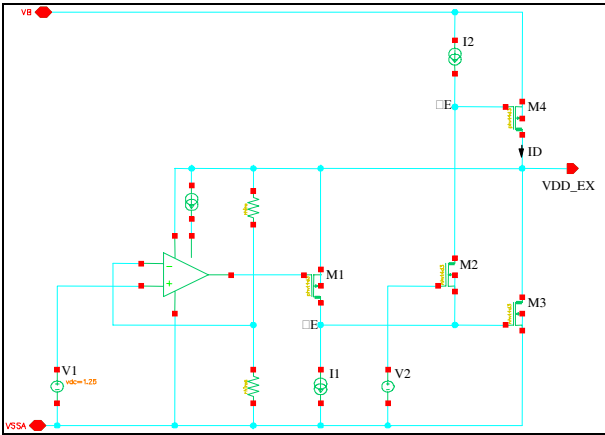


Fig.1. First regulator topology LDO

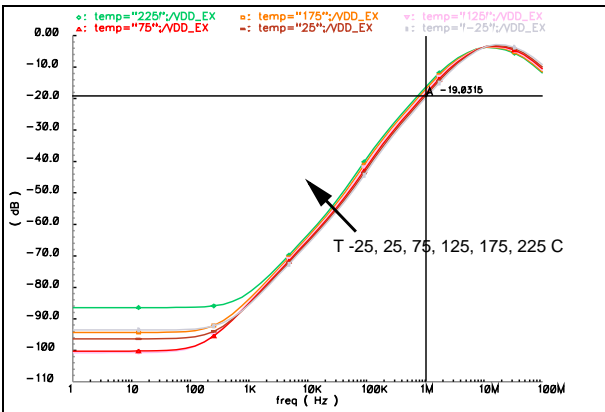


Fig.3 PSRR versus frequency. The parameter is the temperature. First regulator topology LDO

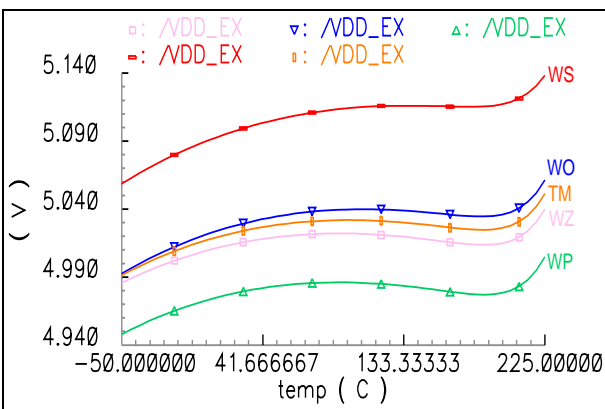


Fig.5 Output Voltage (VDD_EX) versus temperature for different worst cases. First regulator structure LDO.

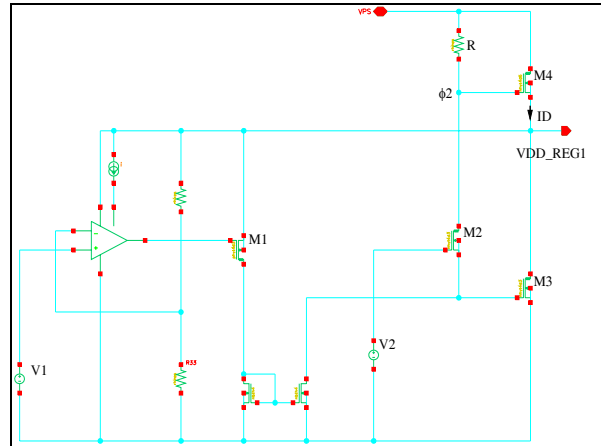


Fig.2 Second regulator topology non LDO.

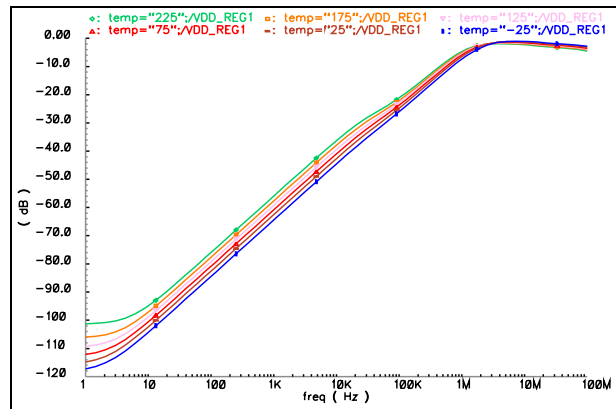


Fig.4 PSRR versus frequency. The parameter is the temperature. Second regulator topology non LDO

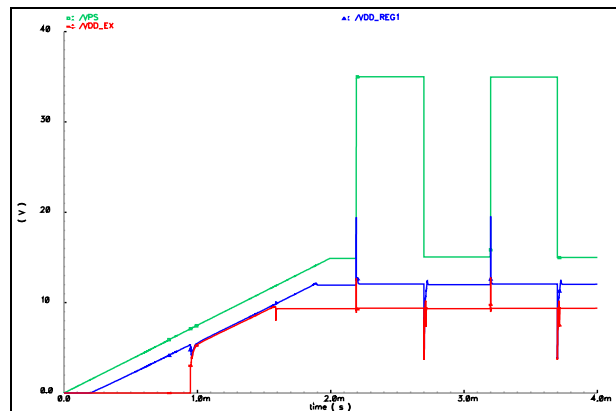


Fig.6. Start-up and step response of the second topology non LDO, The temperature is set to 25°C.

References

[1] V.V. Ivanov and I.M. Filanovsky, "Operational Amplifier Speed and Accuracy Improvement", Kluwer Academic Publishers, 2004.
 [2] J.H. Huijsing, Operational Amplifiers, Kluwer Academic Publishers, 2004.