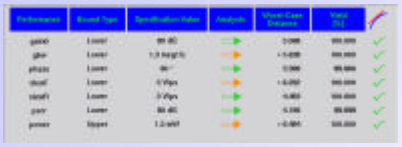
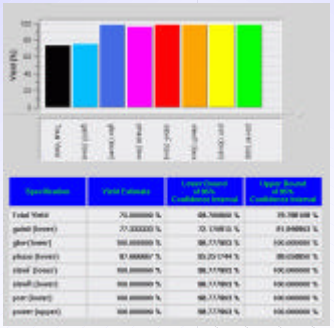
MunEDA

Design for Manufacturability

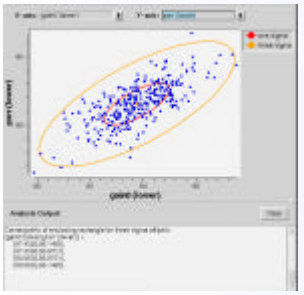
Process Variation & Tolerance Analysis





Worst-case analysis and yield analysis are successfully applied to

- ✓ Very robust mixed-signal circuits
- ✓ Memory devices
- ✓ Cell characterization
- ✓ Parametric yield improvement
- ✓ Mismatch-sensitive circuits

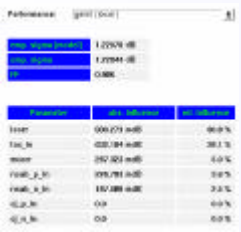


Features

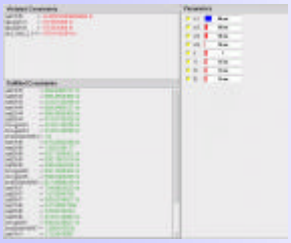
- ✓ Yield estimation including operating conditions (e.g. Temp., Vdd)
- ✓ Performance distributions
- ✓ Margin distributions
- ✓ Parameter influence analysis
- ✓ Parallel simulation on multiple hosts
- ✓ Flexible data export

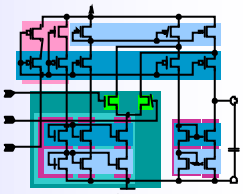
Monte Carlo analysis is productively applied to

- ✓ Yield and mismatch analysis for bandgaps, operational amplifiers, comparators
- ✓ Large circuits with up to 3000 parameters
- ✓ Simulation of extracted view (post-layout)
- ✓ Validation of statistical SPICE models



Structural Constraints & Feasibility



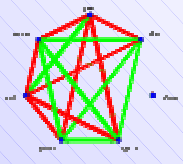


≈ 30 equations
+ 160 inequalities
= 190 sizing rules

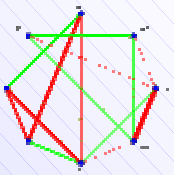
Structural constraints are for example transistor saturation or matching constraints.

- necessary for technically useful designs
- automatically generated ⇒ ease of use
- validated in manual design
- guaranteed in automatic design

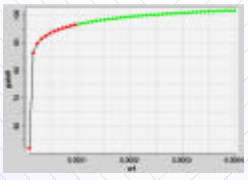
Nominal Design & Design Centering: manually and/or automatically



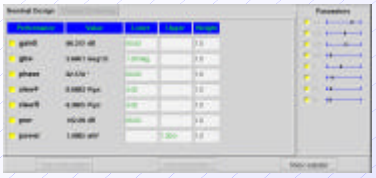
Performance dependency



Parameter redundancy



Parameter Sweep



Automatic nominal optimization

Advanced analysis features make **interactive sizing much faster and less error-prone**.

For automatic sizing, four local and global **optimization engines** are included.

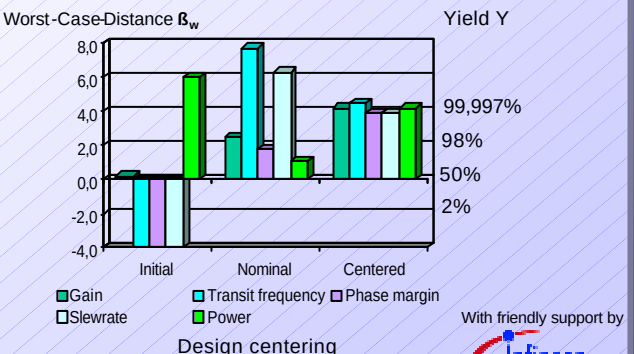
Applied successfully to

- ✓ Operational amplifiers
- ✓ Analog signal processing
- ✓ I/O, digital library cells

For

- ✓ Manual sizing
- ✓ Automatic sizing
- ✓ Yield improvement
- ✓ Compensation of parasitics in extracted view (post-layout)

Nominal diagnosis



Design centering

With friendly support by Infineon