

Medea+ Design Automation Conference

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Results from ANASTASIA+: Top-Down Design Methods for Mixed-Signal Applications

Dr. Ralf Sommer, Infineon Technologies AG, Dept. CL DAT DFA AMF

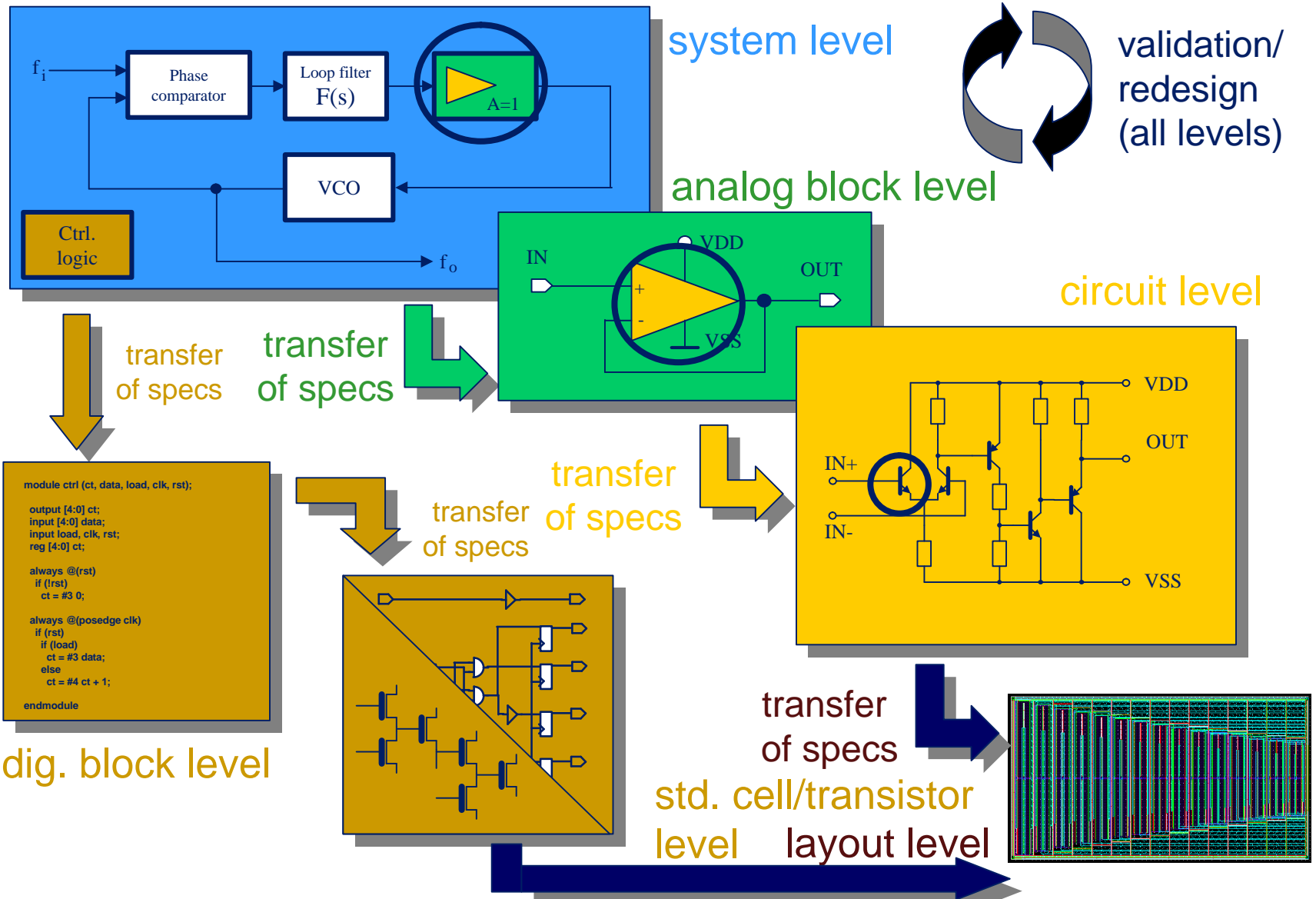


Never stop thinking.

Overview – Results from the ANASTASIA+ Project

- Top-Down Design-Flow
- Symbolic Circuit Analysis and Automated Generation of Behavioral Models
- Reuse-Oriented Analog Design Flow
- Sizing and Yield Optimization (Flow, Techniques & Example)
- A Vision

Top-Down Design-Flow Incorporating Bottom-Up Knowledge and Backannotation of Low-Level Effects



```

module ctrl (ct, data, load, clk, rst);
    output [4:0] ct;
    input [4:0] data;
    input load, clk, rst;
    reg [4:0] ct;

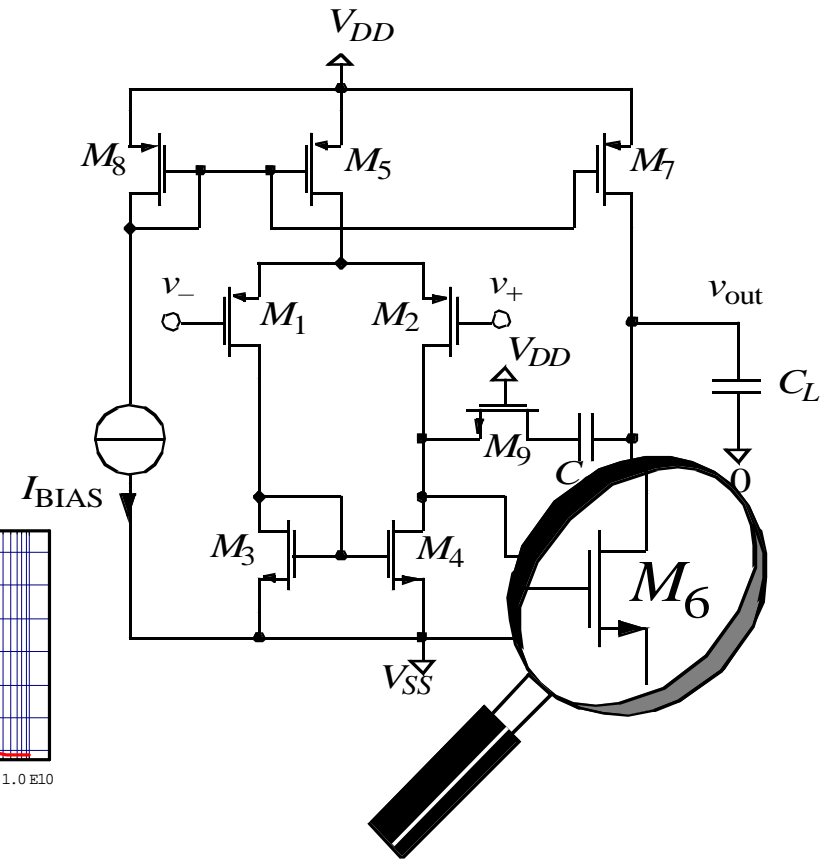
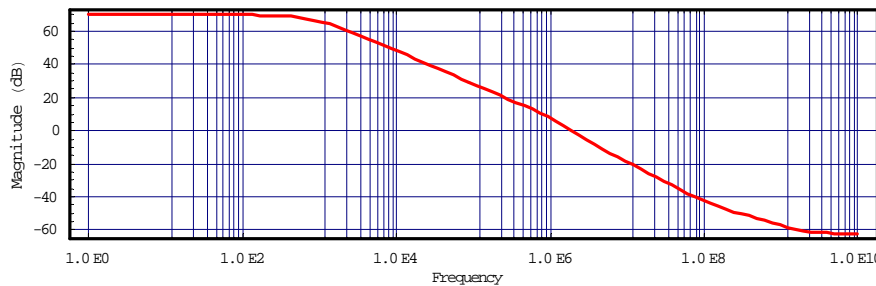
    always @(rst)
        if (rst)
            ct = #3 0;

    always @(posedge clk)
        if (rst)
            if (load)
                ct = #3 data;
            else
                ct = #4 ct + 1;
endmodule
    
```

stop thinking
 ever

Symbolic Analysis

- Insight into circuit behavior – how does the circuit work?
- Why does the circuit *not* work?
- Which elements cause circuit failure?



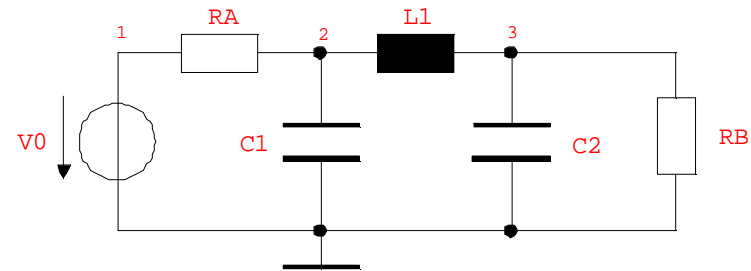
$$H[s] == \frac{gm\$M2 \ gm\$M6 \ VIN1}{(Gds\$M2 + Gds\$M4) (Gds\$M6 + Gds\$M7) + CC \ gm\$M6 \ s}$$

Who Answers these Questions?

How does the circuit work?

How do the elements influence circuit behavior? („Insights“)

Today: Manually by tedious hand-calculations



$$\text{Node 1: } I_{V0} - \frac{v_1 - v_2}{R_A} = 0$$

$$\text{Node 2: } sC_1 v_2 + \frac{v_2 - v_1}{R_A} + \frac{v_2 - v_3}{sL_1} = 0$$

Node 3, and solve them :

$$H(s) = \frac{R_B V_0}{R_A + R_B + sL_1 + s(C_1 + C_2)R_A R_B + s^2 C_1 L_1 R_A + s^2 C_2 L_1 R_B + s^3 C_1 C_2 L_1 R_A R_B}$$

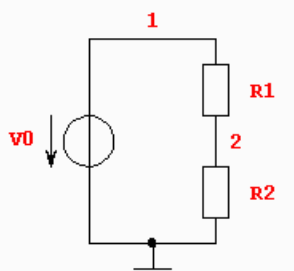
Who Answers these Questions?

How does the circuit work? („Insights“)

Today:
Let
Analog Insydes
do circuit analysis

AnalogInsydes.nb

■ Voltage Divider (Basics)



```
<< AnalogInsydes`
VoltageDivider =
Netlist[
{V0, {1, 0}, V0},
{R1, {1, 2}, R1},
{R2, {2, 0}, R2}
];

eqs = CircuitEquations[VoltageDivider] // DisplayForm

$$\begin{pmatrix} \frac{1}{R1} & -\frac{1}{R1} & 1 \\ -\frac{1}{R1} & \frac{1}{R1} + \frac{1}{R2} & 0 \\ 1 & 0 & 0 \end{pmatrix} \cdot \begin{pmatrix} V\$1 \\ V\$2 \\ I\$V0 \end{pmatrix} == \begin{pmatrix} 0 \\ 0 \\ V0 \end{pmatrix}$$

Solve[eqs, V$2]
{{V$2 →  $\frac{R2 V0}{R1 + R2}$ }}
```

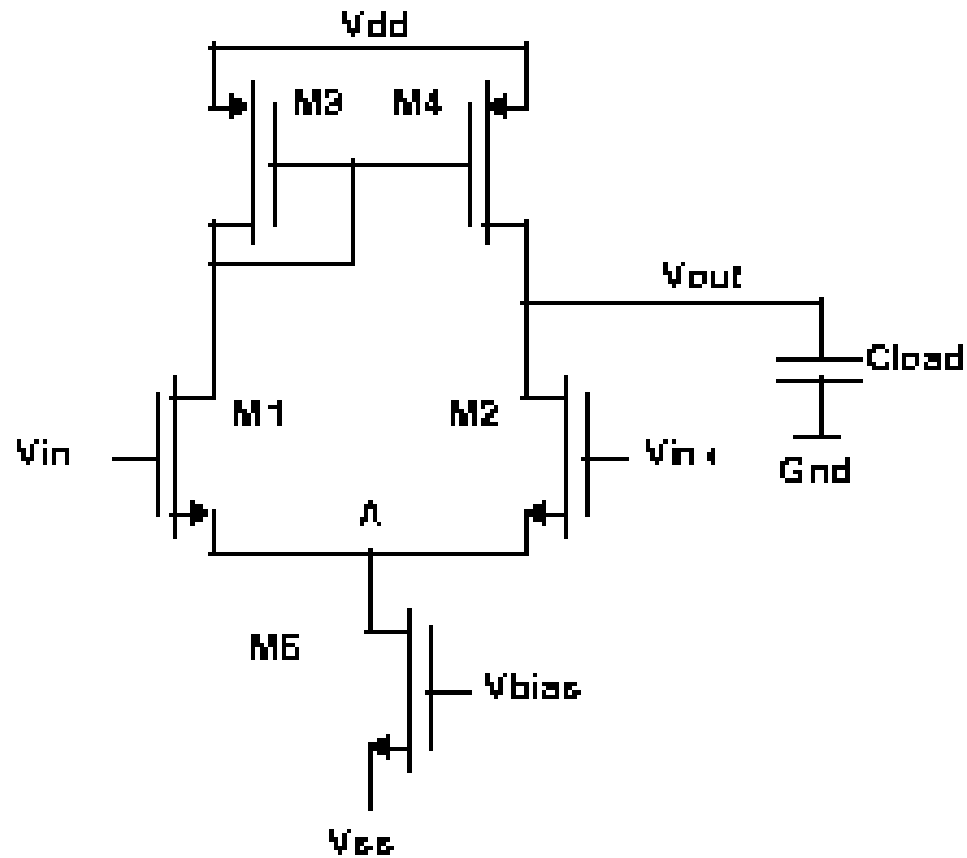
Read the netlist from Composer

Let AI set up equations

Let AI solve equations

100%

Op Amp Schematic - Demo for New Algorithm/Tool



Op Amp Schematic - Real World Example

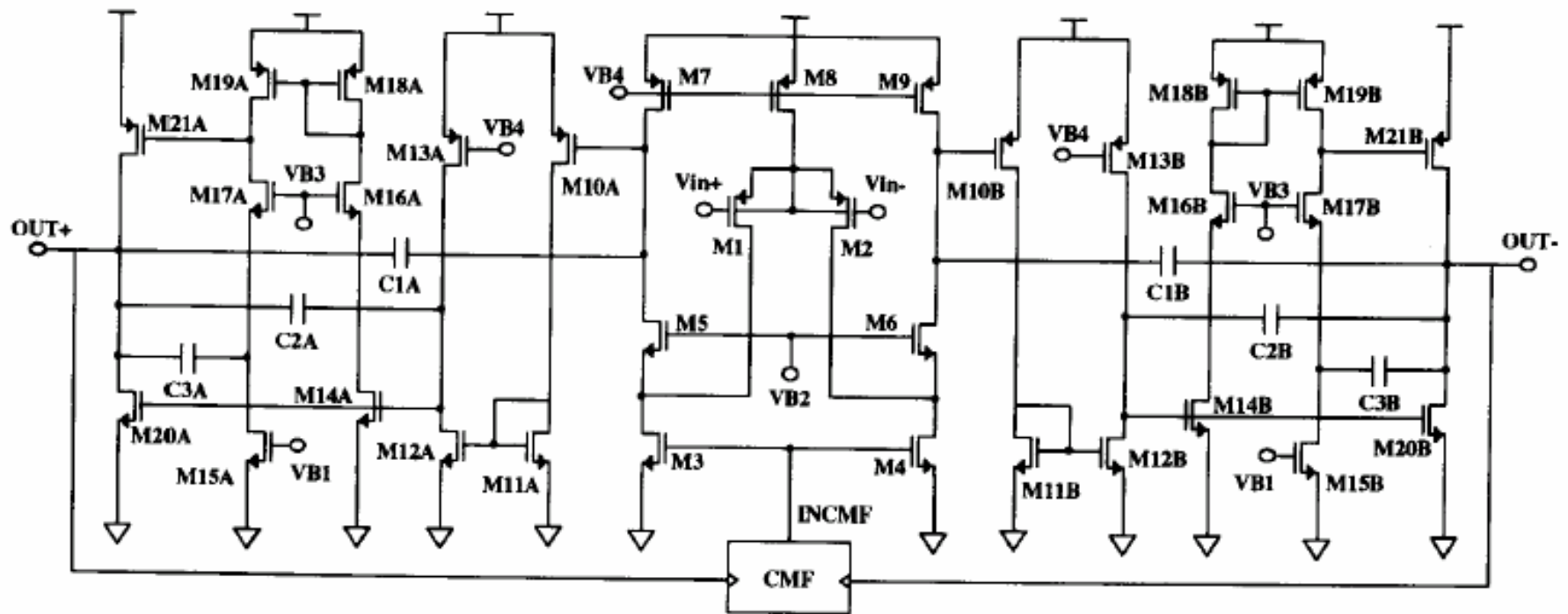
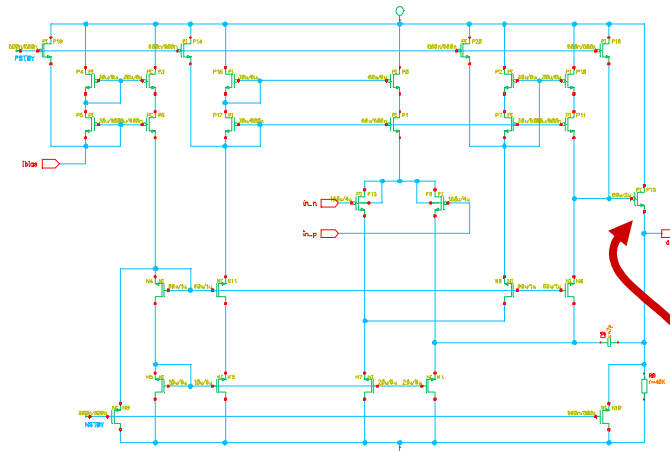


Fig. 4. Overall amplifier schematic.

Folded Cascode CMOS Opamp (C10)

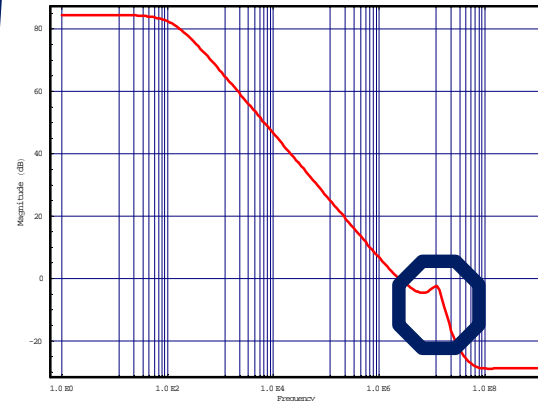
Failure Analysis by Symbolic Analysis (Analog Insydes)



- Resonance peak near 10 MHz: Why?
- Full symbolic transfer function has more than $5 \cdot 10^{19}$ terms
 - ➔ printed $2.5 \cdot 10^{14}$ pages
 - ➔ 25 Giga km books ~ 1 light-day!!!
- Breakthrough: Symbolic approximation

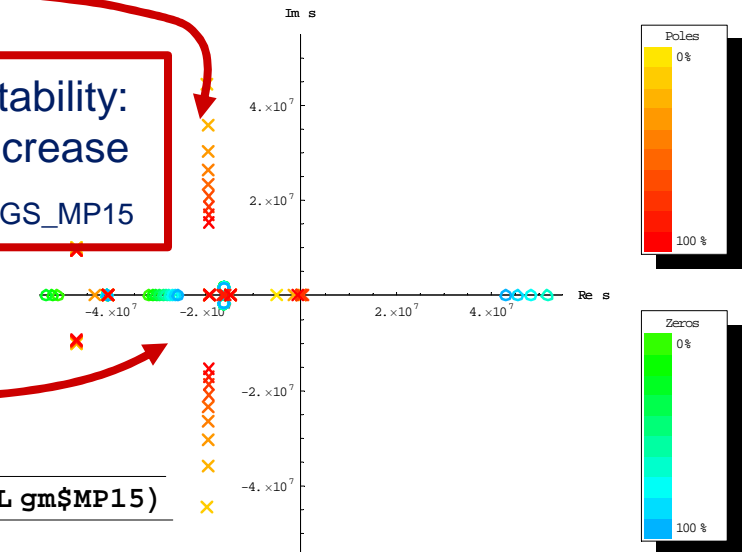
Automated derivation of symbolic expression

here:
parasitic pole pair



Stability:
increase
 C_{GS_MP15}

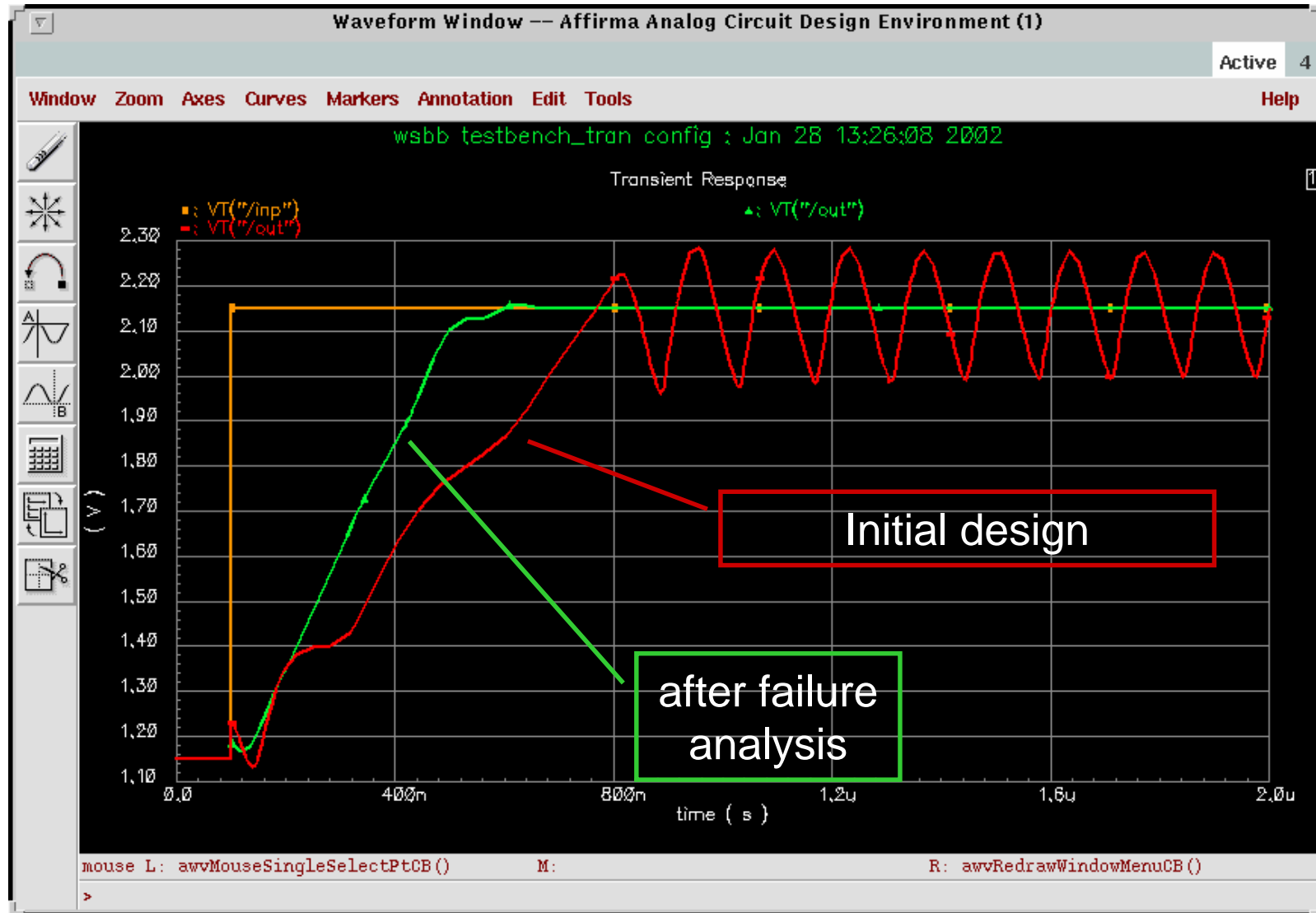
$C_{GS_MP15} = 1.000 \text{ e-12} \dots 1.000 \text{ e-11} \text{ (0\% .. 100\%)}$



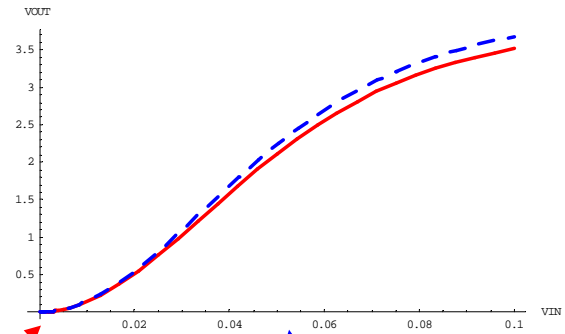
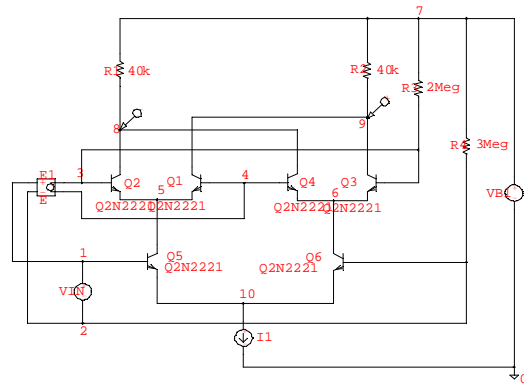
$$-\frac{(CC0 + CL) gm\$MN6}{2 CC0 CL} + \frac{\sqrt{Cgs\$MP15 gm\$MN6} \boxed{Cgs\$MP15} (CC0 + CL)^2 gm\$MN6 - 4 CC0^2 CL gm\$MP15}{2 CC0 Cgs\$MP15 CL}$$

stop thinking
ever

Failure Analysis: Transient Response (Unity Gain)



Automated Generation of Behavioral Models



nonlinear model / equations

$$\begin{aligned}
 & \{ I_{SBC\$Q5} + I_{SBE\$Q5} + I_{\$VIN} == 0, -I_{SBE\$Q5} - I_{SBE\$Q6} == -I1, \\
 & I_{SBC\$Q6} + I_{SBE\$Q6} - I_{\$VIN} \cdot \frac{V_{\$2} - V_{\$7}}{R4} == 0, I_{SBC\$Q2} + I_{SBC\$Q3} + I_{SBE\$Q2} + I_{SBE\$Q3} + I_{\$E1} \cdot \frac{V_{\$3} - V_{\$7}}{R3} == 0, \\
 & I_{SBC\$Q1} + I_{SBC\$Q4} + I_{SBE\$Q1} + I_{SBE\$Q4} - I_{\$E1} == 0, -I_{SBC\$Q5} - I_{SBE\$Q1} - I_{SBE\$Q2} == 0, -I_{SBC\$Q6} - I_{SBE\$Q3} - I_{SBE\$Q4} == 0, \\
 & I_{\$VB1} \cdot \frac{-V_{\$2} + V_{\$7}}{R4} + \frac{-V_{\$3} + V_{\$7}}{R3} + \frac{V_{\$7} - V_{\$8}}{R1} + \frac{V_{\$7} - V_{\$9}}{R2} == 0, -I_{SBC\$Q2} - I_{SBC\$Q4} + \frac{-V_{\$7} + V_{\$8}}{R1} == 0, -I_{SBC\$Q1} - I_{SBC\$Q3} + \frac{-V_{\$7} + V_{\$9}}{R2} == 0, \\
 & E1 (-V_{\$1} + V_{\$2}) + V_{\$3} - V_{\$4} == 0, V_{\$7} == V_{\$1}, I_{SBC\$Q5} == -\left(-1 + E^{\frac{V_{\$1} - V_{\$10}}{V_T}}\right) I_{SSQ5} + \frac{(1 + BR\$Q5) \left(-1 + E^{\frac{V_{\$1} - V_{\$5}}{V_T}}\right) I_{SSQ5}}{BR\$Q5}, \\
 & I_{SBE\$Q5} == \frac{(1 + BF\$Q5) \left(-1 + E^{\frac{V_{\$1} - V_{\$10}}{V_T}}\right) I_{SSQ5}}{BF\$Q5} + \left(1 - E^{\frac{V_{\$1} - V_{\$5}}{V_T}}\right) I_{SSQ5}, I_{SBC\$Q2} == -\left(-1 + E^{\frac{V_{\$3} - V_{\$5}}{V_T}}\right) I_{SSQ2} + \frac{(1 + BR\$Q2) \left(-1 + E^{\frac{V_{\$3} - V_{\$8}}{V_T}}\right) I_{SSQ2}}{BR\$Q2}, \\
 & I_{SBE\$Q2} == \frac{(1 + BF\$Q2) \left(-1 + E^{\frac{V_{\$3} - V_{\$5}}{V_T}}\right) I_{SSQ2}}{BF\$Q2} + \left(1 - E^{\frac{V_{\$3} - V_{\$8}}{V_T}}\right) I_{SSQ2}, I_{SBC\$Q1} == -\left(-1 + E^{\frac{V_{\$4} - V_{\$5}}{V_T}}\right) I_{SSQ1} + \frac{(1 + BR\$Q1) \left(-1 + E^{\frac{V_{\$4} - V_{\$9}}{V_T}}\right) I_{SSQ1}}{BR\$Q1}, \\
 & I_{SBE\$Q1} == \frac{(1 + BF\$Q1) \left(-1 + E^{\frac{V_{\$4} - V_{\$5}}{V_T}}\right) I_{SSQ1}}{BF\$Q1} + \left(1 - E^{\frac{V_{\$4} - V_{\$9}}{V_T}}\right) I_{SSQ1}, I_{SBC\$Q4} == -\left(-1 + E^{\frac{V_{\$4} - V_{\$6}}{V_T}}\right) I_{SSQ4} + \frac{(1 + BR\$Q4) \left(-1 + E^{\frac{V_{\$4} - V_{\$8}}{V_T}}\right) I_{SSQ4}}{BR\$Q4}, \\
 & I_{SBE\$Q4} == \frac{(1 + BF\$Q4) \left(-1 + E^{\frac{V_{\$4} - V_{\$6}}{V_T}}\right) I_{SSQ4}}{BF\$Q4} + \left(1 - E^{\frac{V_{\$4} - V_{\$8}}{V_T}}\right) I_{SSQ4}, I_{SBC\$Q3} == -\left(-1 + E^{\frac{V_{\$3} - V_{\$6}}{V_T}}\right) I_{SSQ3} + \frac{(1 + BR\$Q3) \left(-1 + E^{\frac{V_{\$3} - V_{\$9}}{V_T}}\right) I_{SSQ3}}{BR\$Q3}, \\
 & I_{SBE\$Q3} == \frac{(1 + BF\$Q3) \left(-1 + E^{\frac{V_{\$3} - V_{\$6}}{V_T}}\right) I_{SSQ3}}{BF\$Q3} + \left(1 - E^{\frac{V_{\$3} - V_{\$9}}{V_T}}\right) I_{SSQ3}, I_{SBC\$Q6} == -\left(-1 + E^{\frac{V_{\$10} - V_{\$2}}{V_T}}\right) I_{SSQ6} + \frac{(1 + BR\$Q6) \left(-1 + E^{\frac{V_{\$2} - V_{\$6}}{V_T}}\right) I_{SSQ6}}{BR\$Q6}, \\
 & I_{SBE\$Q6} == \frac{(1 + BF\$Q6) \left(-1 + E^{\frac{V_{\$10} - V_{\$2}}{V_T}}\right) I_{SSQ6}}{BF\$Q6} + \left(1 - E^{\frac{V_{\$2} - V_{\$6}}{V_T}}\right) I_{SSQ6}, V_{\$1} - V_{\$2} == VIN, V_{\$8} - V_{\$9} + V_{\$OUT} == 0 \}
 \end{aligned}$$

$$I1 \left(\frac{\left(1 + e^{\frac{VIN1 + VIN2}{VT}}\right) R1 - \left(e^{VIN1/VT} + e^{VIN2/VT}\right) R2}{\left(1 + e^{VIN1/VT}\right) \left(1 + e^{VIN2/VT}\right)} \right)$$

approximation

insight

original-DAE

behavioral model generation

stop thinking
ever

Analog & RF specified data

- noise
- distortion
- signal-to-noise
- signal-to-distortion
- power supply rejection ratio
- common mode rejection ratio
- slew rate (linear dominated)
- slew rate (nonlinear dynamic)
- bandwidth
- gain [F(frequency, load, bias,...)]
- phase margin
- gain margin
- offset
- resolution
- spurious free dynamic range
- noise figure
- IP2
- IP3
- 1dB compression point
- phase noise
- bandwidth
- gain @ frequency
- gain over load

State-of-the-Art : Symbolic analysis

Available for industrial application
(based on linear analysis)

Topic of research/under development
(nonlinear analysis)

Challenges

Analog Circuit ~~Synthesis~~ Sizing

Knowledge based

- Basic idea: solve circuit design equations
(W, L, R, C,...) = F (gain, bandwidth, ...)
- Examples: IDAC, OASYS, MIDAS

Optimization - equation based

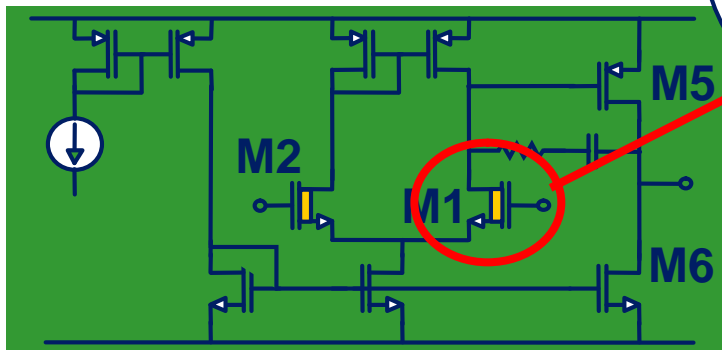
- Basic idea: run optimizer over simplified circuit behavior
equations (gain, BW) = F (W, L, R,...)
- Examples: DONALD & ISAAC

Optimization - 'Spice' based (brute force)

- Basic idea: optimization based on Spice runs
- Examples: ASTRX / OBLX , some commercial tools

Sizing, Yield Analysis, and Design Centering

stop thinking
never



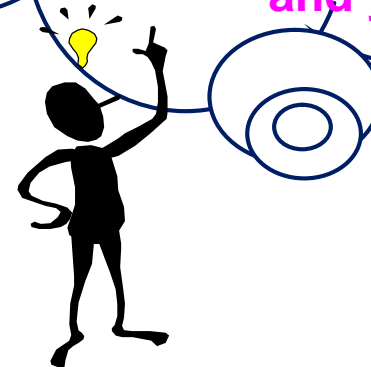
I know my **topology and specs**
I know how to measure my specs
with SPICE (testbench, characterization)

I know how the **circuit works**

I let the sizing engine determine **W1,
W2, W3, W4...**

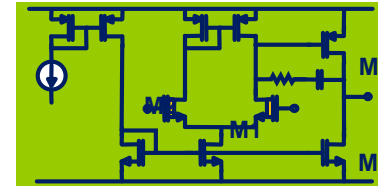
and minimize area and power

and **optimize robustness
and yield!**



Sizing and Optimization Flow

Circuit Specs



Choose a circuit topology

Configure testbenches

Set up sizing constraints

$M2.w = M1.w,$
 $M2.l = M1.l, \dots$

$A0 > 80 \text{ dB}, PM > 60,$
 $\text{Slewrate} > 1 \text{ V}/\mu\text{s}, \dots$

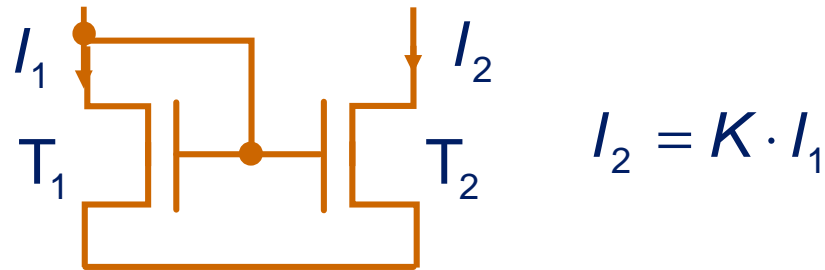
Define circuit goals (characterization)

Size the design (nominal)

Analyze and optimize yield

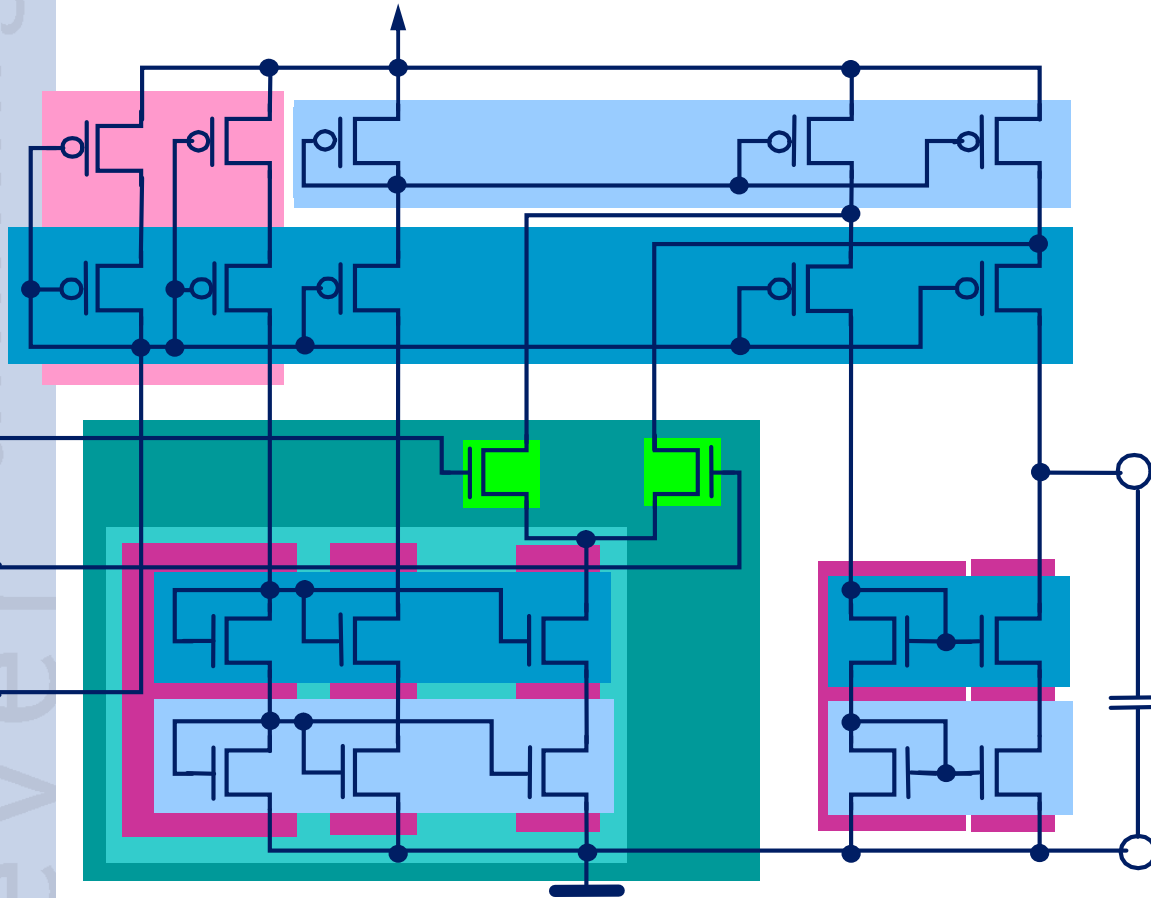
Sized Schematic...
To Layout

Research Result: Sizing Rules (Current Mirror)



	geometrical	electrical
function	$L_1 = L_2 \quad (1)$ $K = \frac{W_2}{W_1} \quad (2)$	$ v_{ds2} - v_{ds1} \leq \Delta V_{ds,max} \quad (9)$ $v_{ds1,2} - (v_{gs1,2} - V_{th1,2}) \geq V_{sat\ min} \quad (10,11)$ $v_{ds1,2} \geq 0; \quad v_{gs1,2} - V_{th1,2} \geq 0 \quad (12-15)$
robustness	$L_{1,2} \cdot W_{1,2} \geq A_{min} \quad (3,4)$ $L_{1,2} \geq L_{min} \quad (5,6)$ $W_{1,2} \geq W_{min} \quad (7,8)$	$ v_{gs} - V_{th1,2} \geq V_{gs\ min} \quad (16,17)$

Structural analysis: Folded-Cascode-OpAmp

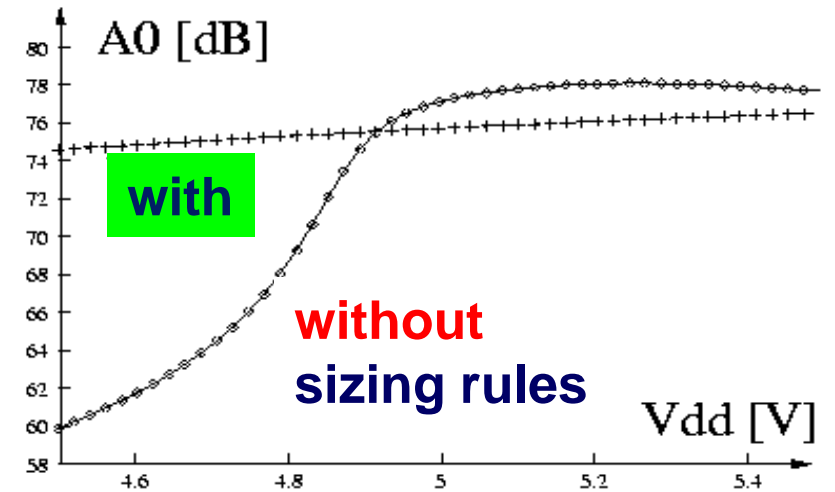
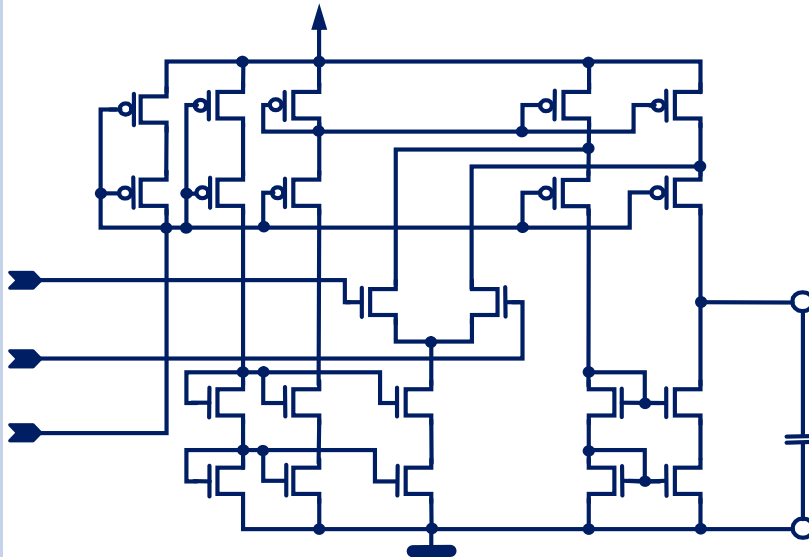


- Voltage ref 1
- Current mirror load
- Simple CM
- Levelshifter
- Differential pair

- 4-transistor-CM
- CM(-bank)
- Levelshifter(-bank)
- Cascode-CM
- Cascode-CM -bank
- Differential stage (Type 4)

\approx 30 equations
 + 160 inequalities
 = 190 sizing constraints

Sizing using Sizing Rules



Sizing Rules / Constraints	without	with
# violated sizing rules	7	0
# simulations (incl. sensitivity)	126	45
# violated		no

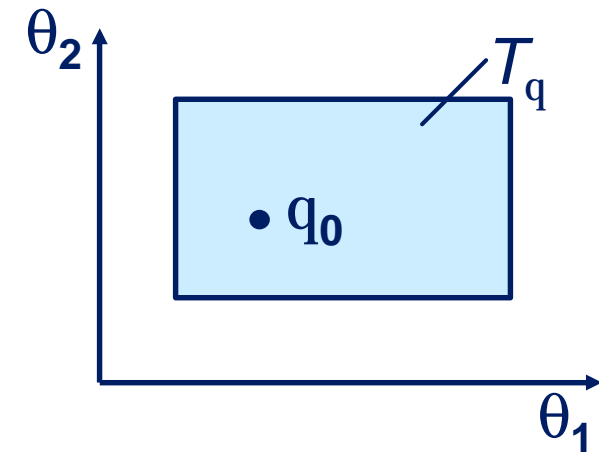
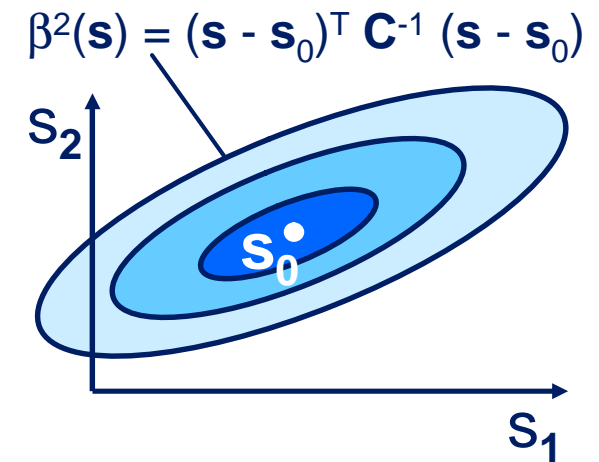
Physically meaningful element sizing

Shorten design time

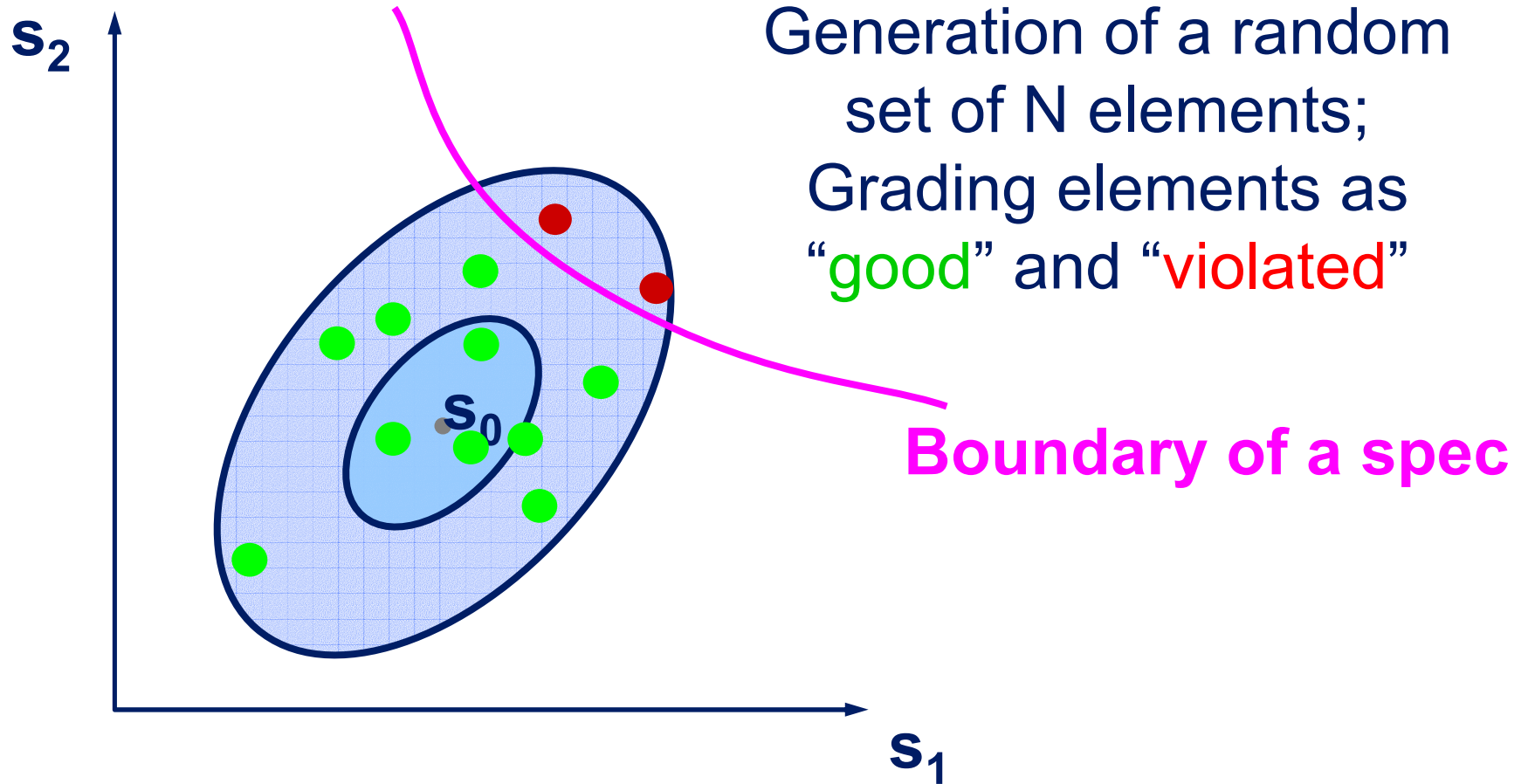
Improved robustness

Definitions for Design Centering

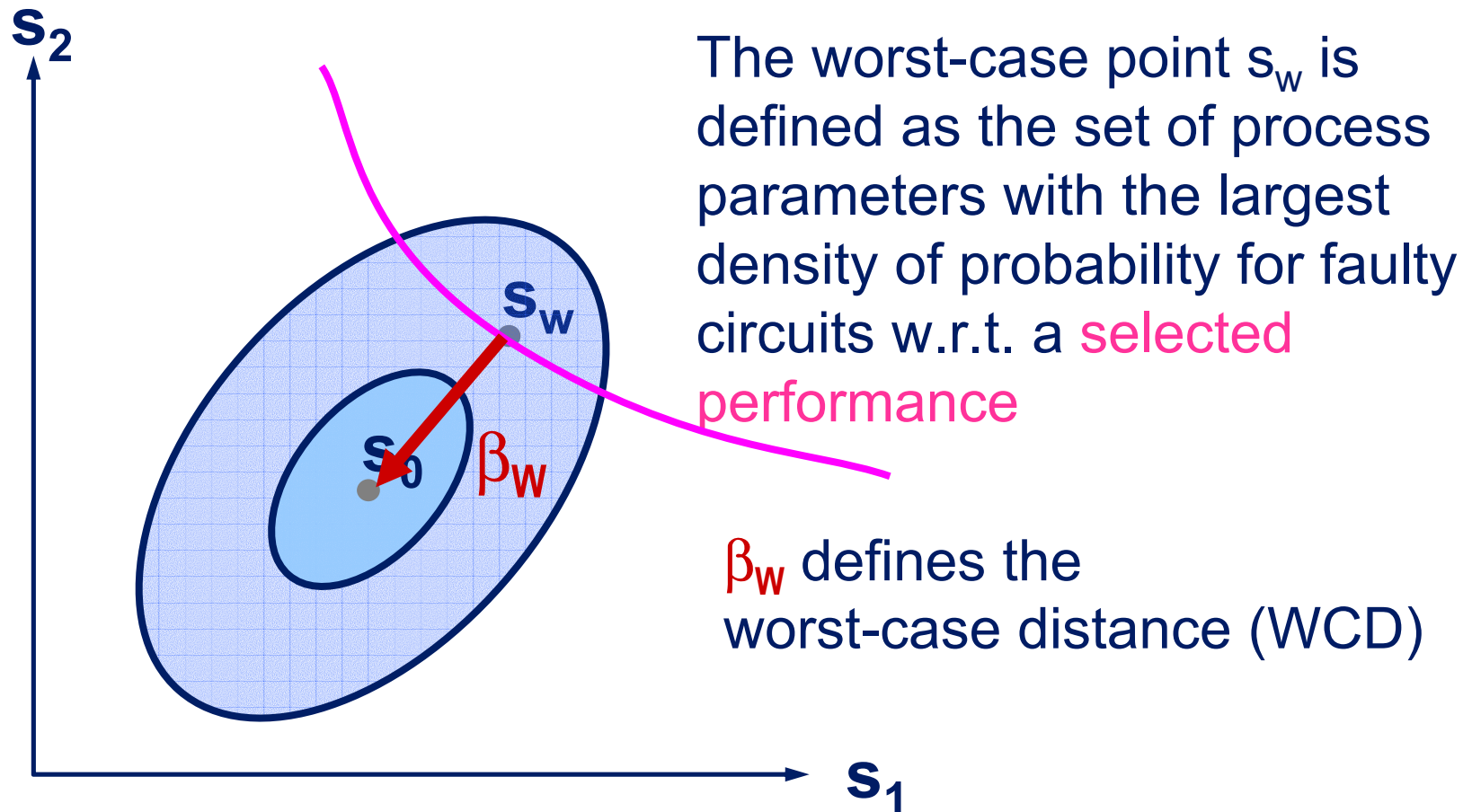
- **Design parameters** d (e.g. width, length):
 - Can be tuned by the circuit designer
- **Statistical parameters** s (e.g. tox):
 - Describe the process variations
- **Operational parameters** q (e.g. V_{DD}):
 - Describe the operating conditions
- **Specifications** f (e.g. gain, bandwidth, input impedance, area ...)



Monte-Carlo Analysis

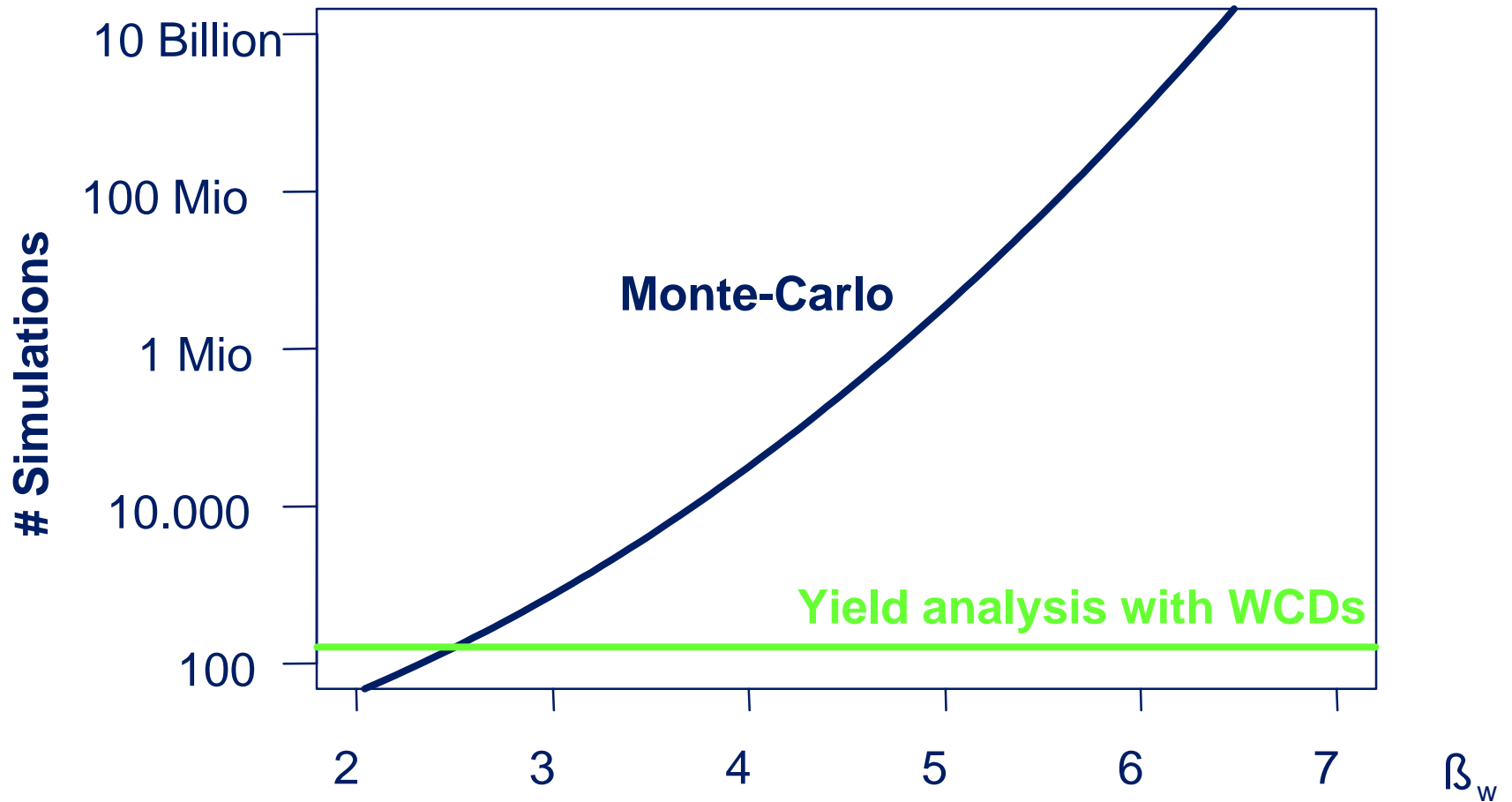


Worst-Case Point s_w and Worst-Case Distance β_w



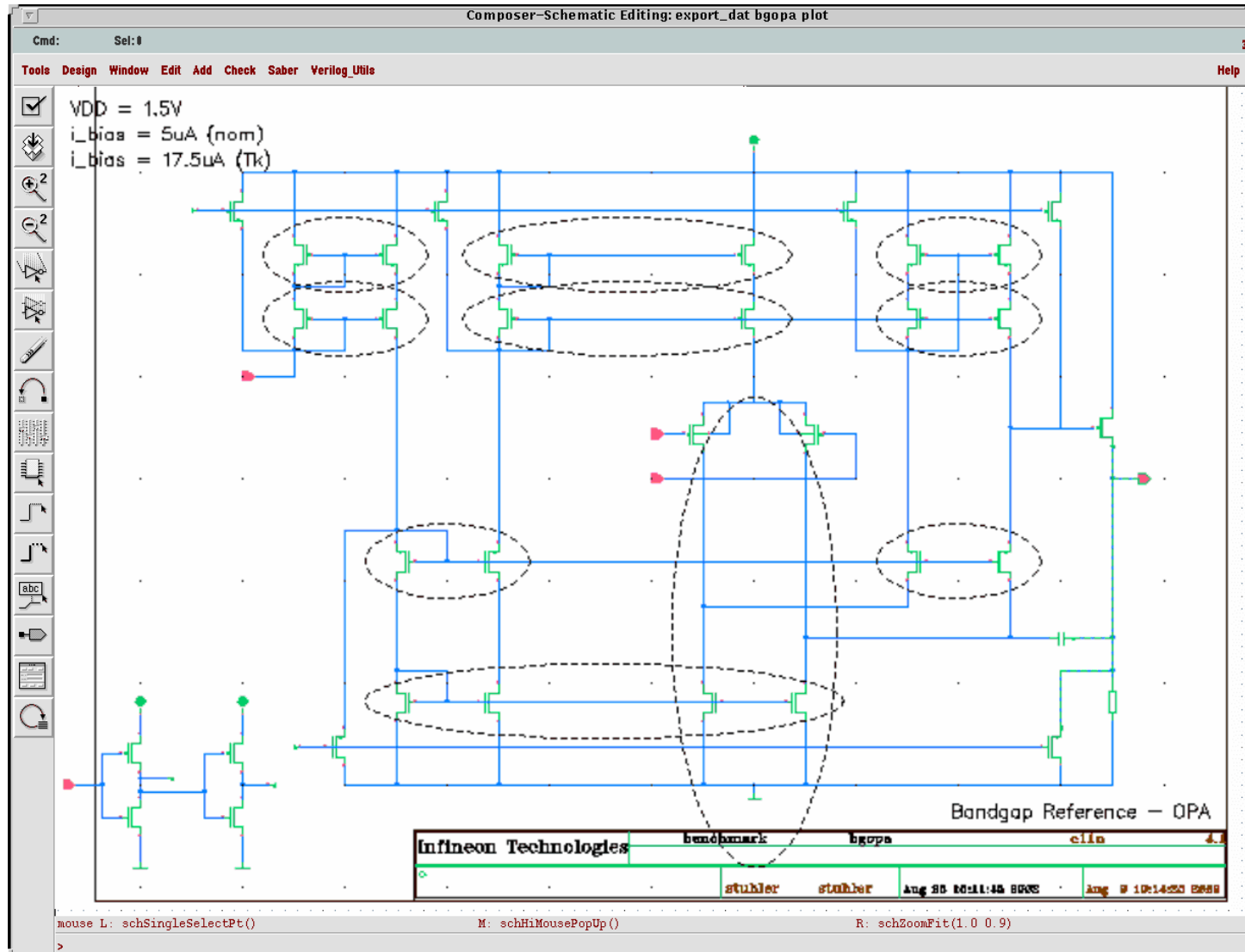
β_w	-1	0	1	2	3
\bar{Y}	32.3%	50.0%	67.7%	84.1%	99.9%

Cost Comparison: Yield Analysis with WCD vs. Monte-Carlo



Advantage WCD: more efficient and accurate than MC for yield > 3s

Benchmark Example: CMOS Folded-Cascode Amplifier



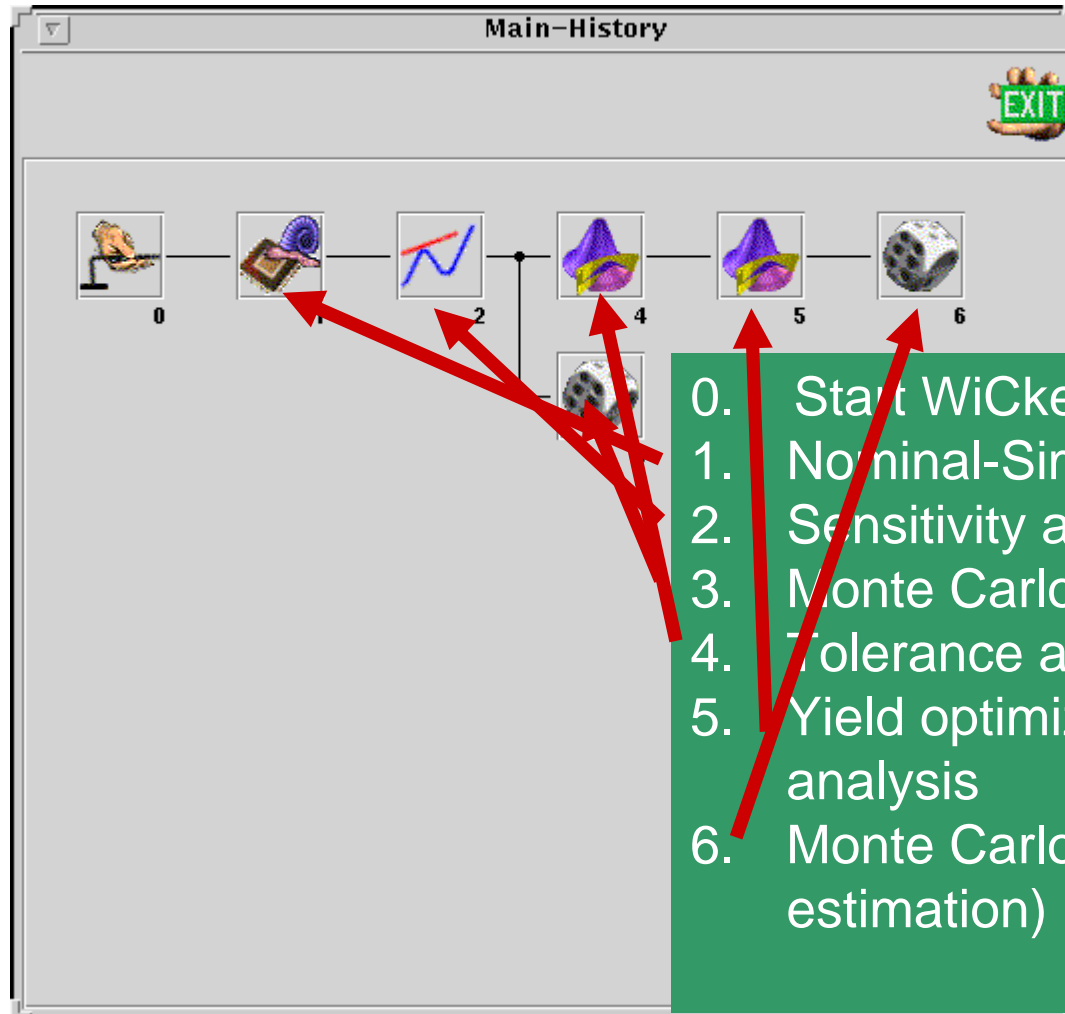
Tasks

1. Starting point – nominal design
 - Nominal sizing using NeoCircuit 1.2 (NeoLinear Inc.)
 - 4 corners: LVLT, LVHT, HVLT, HVHT
 - LV = 1,4V, HV = 1.6V, nominal = 1.5V,
 - LT = 0°C, HT = 50°C, nominal = 27°C
 - Operating regions of transistors as constraints (specs must be satisfied for all corners)
2. Analysis und optimization using WiCkeD (MunEDA)
 - Yield analysis of nominal sized circuit : 96% = 1.7σ -design
 - Goal: Optimize yield using WiCkeD

Specifications & Performances of Nominal Design (NeoCircuit)

Performance	Specification	Initial
Supply voltage	1.5 V	
Load	10 M Ω 10 pF	
DC Gain	> 80 dB (maximize!)	96.75 dB
Gain margin	> 10	10.73
Phase margin	> 60°	74.8°
Unity-gain frequency	> 1 MHz (maximize!)	2.55 MHz
Slew rate	> 0.5 V/ μ s (maximize!)	1.61 V/ μ s
Overshoot	< 10 mV	0 mV
Power	< 300 μ W (minimize!)	80.6 μ W

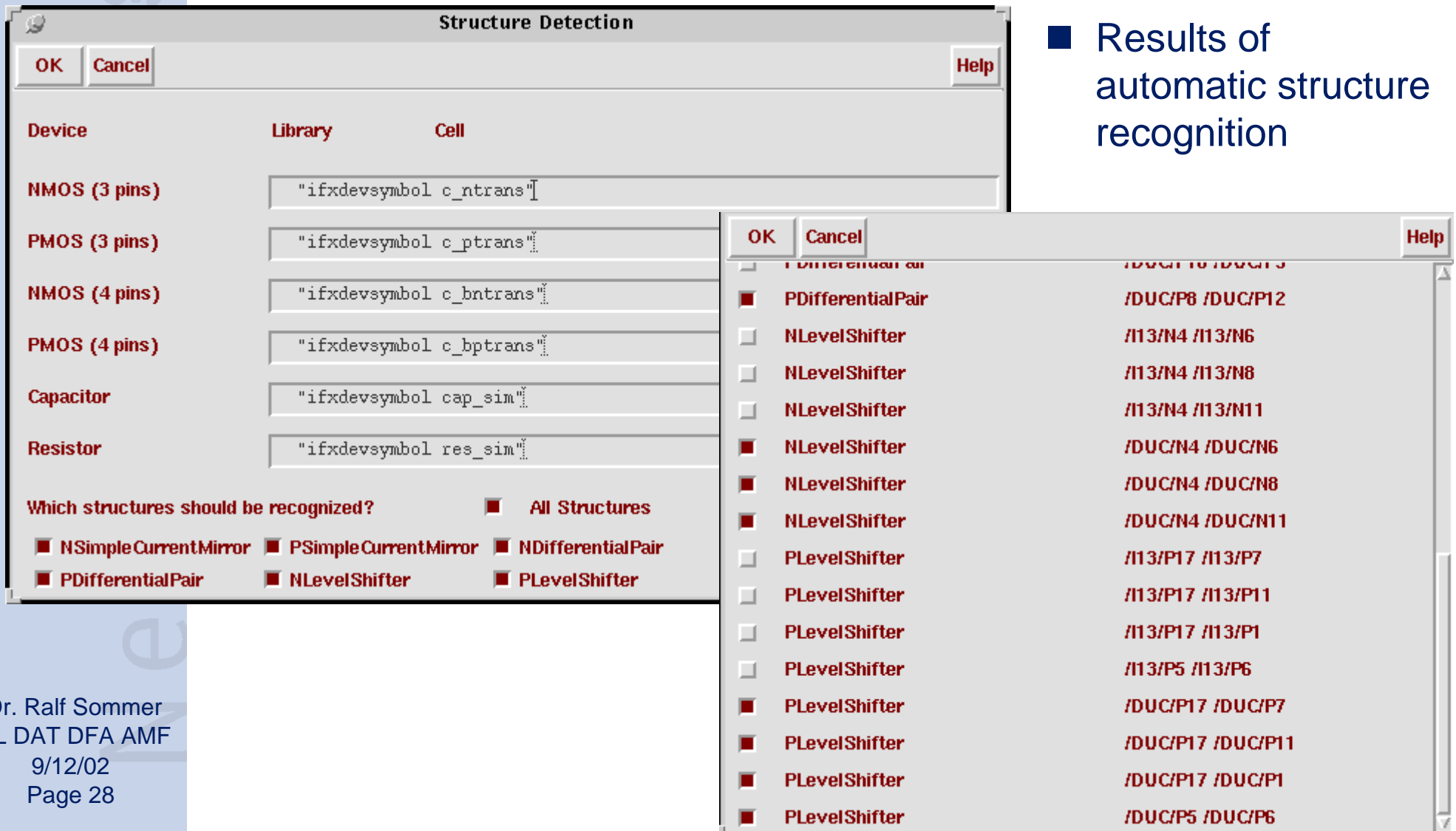
Analysis and Optimization Flow



0. Start WiCkED
1. Nominal-Simulation
2. Sensitivity analysis
3. Monte Carlo (yield of nominal design)
4. Tolerance analysis (WCDs)
5. Yield optimization based on tolerance analysis
6. Monte Carlo (verification of yield estimation)

Automatic Structure Recognition Results

- Results of automatic structure recognition



The screenshot shows the 'Structure Detection' dialog box with the following content:

Device	Library	Cell
NMOS (3 pins)	"ifxdevsymbol c_ntrans"	
PMOS (3 pins)	"ifxdevsymbol c_ptrans"	
NMOS (4 pins)	"ifxdevsymbol c_bntrans"	
PMOS (4 pins)	"ifxdevsymbol c_bptrans"	
Capacitor	"ifxdevsymbol cap_sim"	
Resistor	"ifxdevsymbol res_sim"	

Which structures should be recognized? All Structures

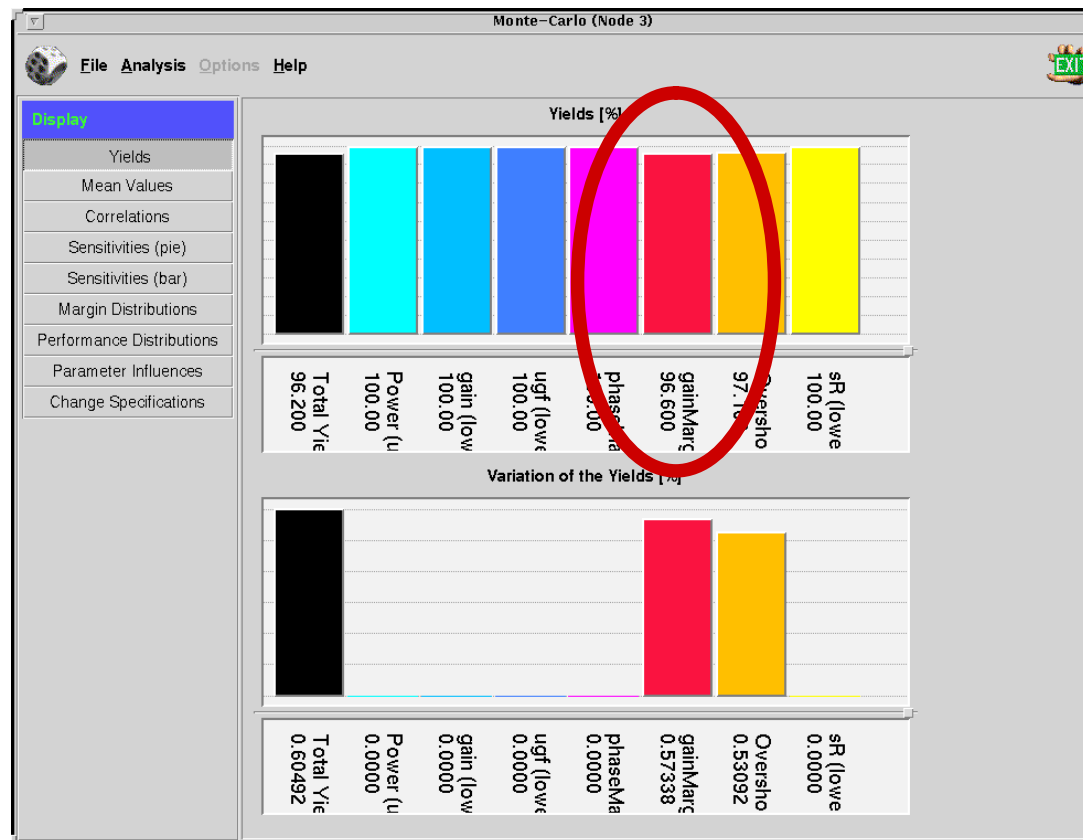
NSimpleCurrentMirror
 PSimpleCurrentMirror
 NDifferentialPair
 PDifferentialPair
 NLevelShifter
 PLevelShifter

The results list is as follows:

Structure	Path
<input checked="" type="checkbox"/> PDifferentialPair	/DUC/P8 /DUC/P12
<input type="checkbox"/> NLevelShifter	/I13/N4 /I13/N6
<input type="checkbox"/> NLevelShifter	/I13/N4 /I13/N8
<input type="checkbox"/> NLevelShifter	/I13/N4 /I13/N11
<input checked="" type="checkbox"/> NLevelShifter	/DUC/N4 /DUC/N6
<input checked="" type="checkbox"/> NLevelShifter	/DUC/N4 /DUC/N8
<input checked="" type="checkbox"/> NLevelShifter	/DUC/N4 /DUC/N11
<input type="checkbox"/> PLevelShifter	/I13/P17 /I13/P7
<input type="checkbox"/> PLevelShifter	/I13/P17 /I13/P11
<input type="checkbox"/> PLevelShifter	/I13/P17 /I13/P1
<input type="checkbox"/> PLevelShifter	/I13/P5 /I13/P6
<input checked="" type="checkbox"/> PLevelShifter	/DUC/P17 /DUC/P7
<input checked="" type="checkbox"/> PLevelShifter	/DUC/P17 /DUC/P11
<input checked="" type="checkbox"/> PLevelShifter	/DUC/P17 /DUC/P1
<input checked="" type="checkbox"/> PLevelShifter	/DUC/P5 /DUC/P6

Yield Analysis of Nominal Design by Monte Carlo

- MC Analysis of Nominal Design → 96% yield, dominated by gain margin
Remark: Nominal design is quite a good starting point!



Determination of WCDs in Nominal Design

thinking



Tolerance analysis

Advantage: more efficient and accurate than MC for yield $> 3\sigma$

Tolerance Diagnosis (Node 4)
EXIT

File Masking Simulation Options Help

Find Feasible Point

Find Feasible Solution

Explore Dependencies

Parameter Dependency

WCD Dependency

Relevant Parameters

Predict Changes

Predict Delta

Parameter Values

Change WP15 by delta: 0.00000

WCD Values

Reset Parameters

Tolerance Analysis (Node 4)
EXIT

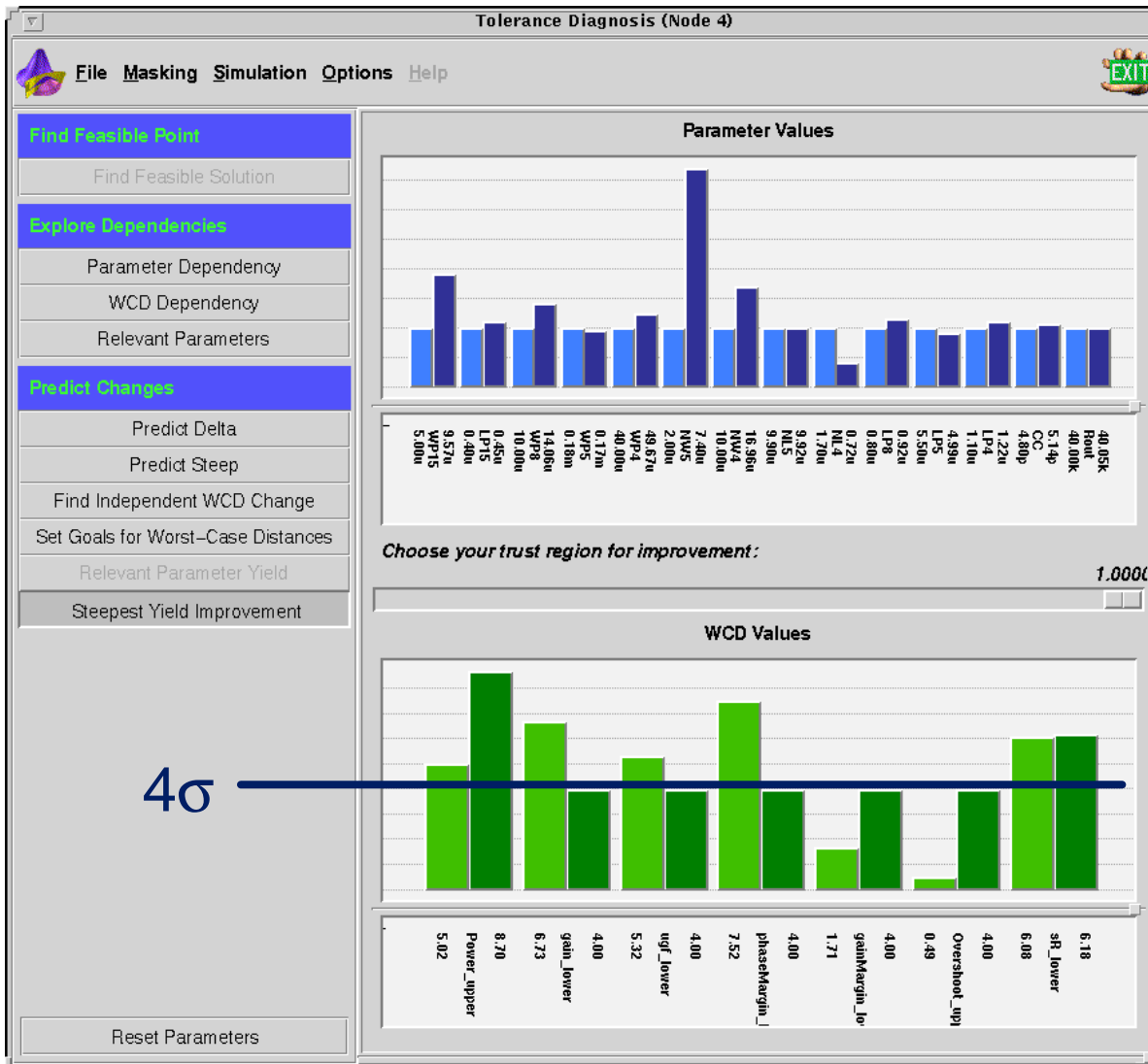
File Analysis Options

Performance	Bound Type	Specification Value	Analysis	Worst-Case Distance	Yield
Power	Upper	300 u	→	(5.020)	(100.000) ✓
gain	Lower	80	→	(6.727)	(100.000) ✓
ugf	Lower	1 meg	→	(5.321)	(100.000) ✓
phaseMargin	Lower	60	→	(7.520)	(100.000) ✓
gainMargin	Lower	10	→	1.706	95.603 ✓
Overshoot	Upper	10 m	→	0.569	71.525 ✓
sR	Lower	500 k	→	(5.050)	(100.000) ✓

All analyses finished.

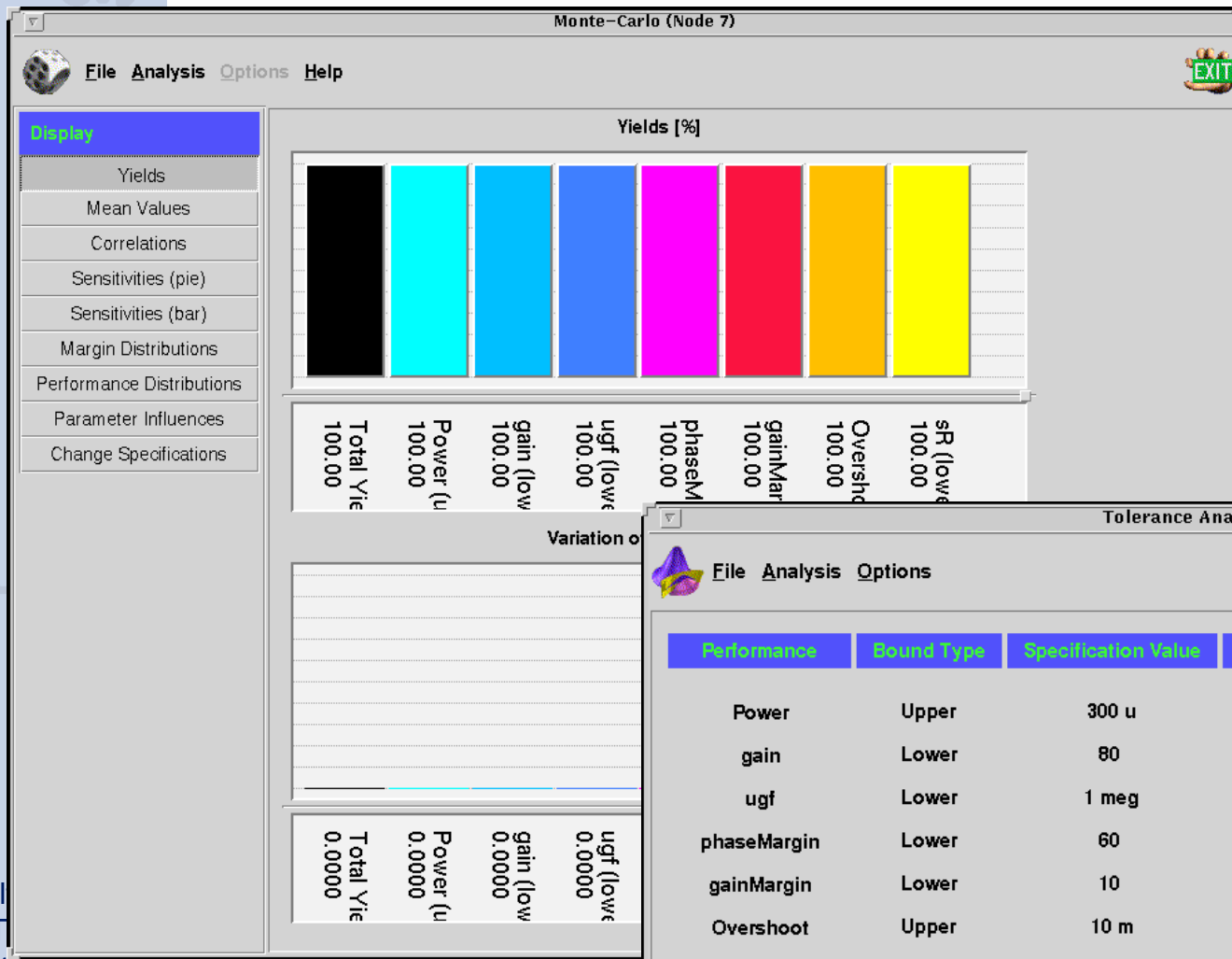
Design Centering based on Linearized Performance Model using WCDs (automatic/manual)

stop thinking
never



- all WCDs normalized
- New yield estimation: ~ 100% (4σ)!

Verification of Centered Design by Monte Carlo



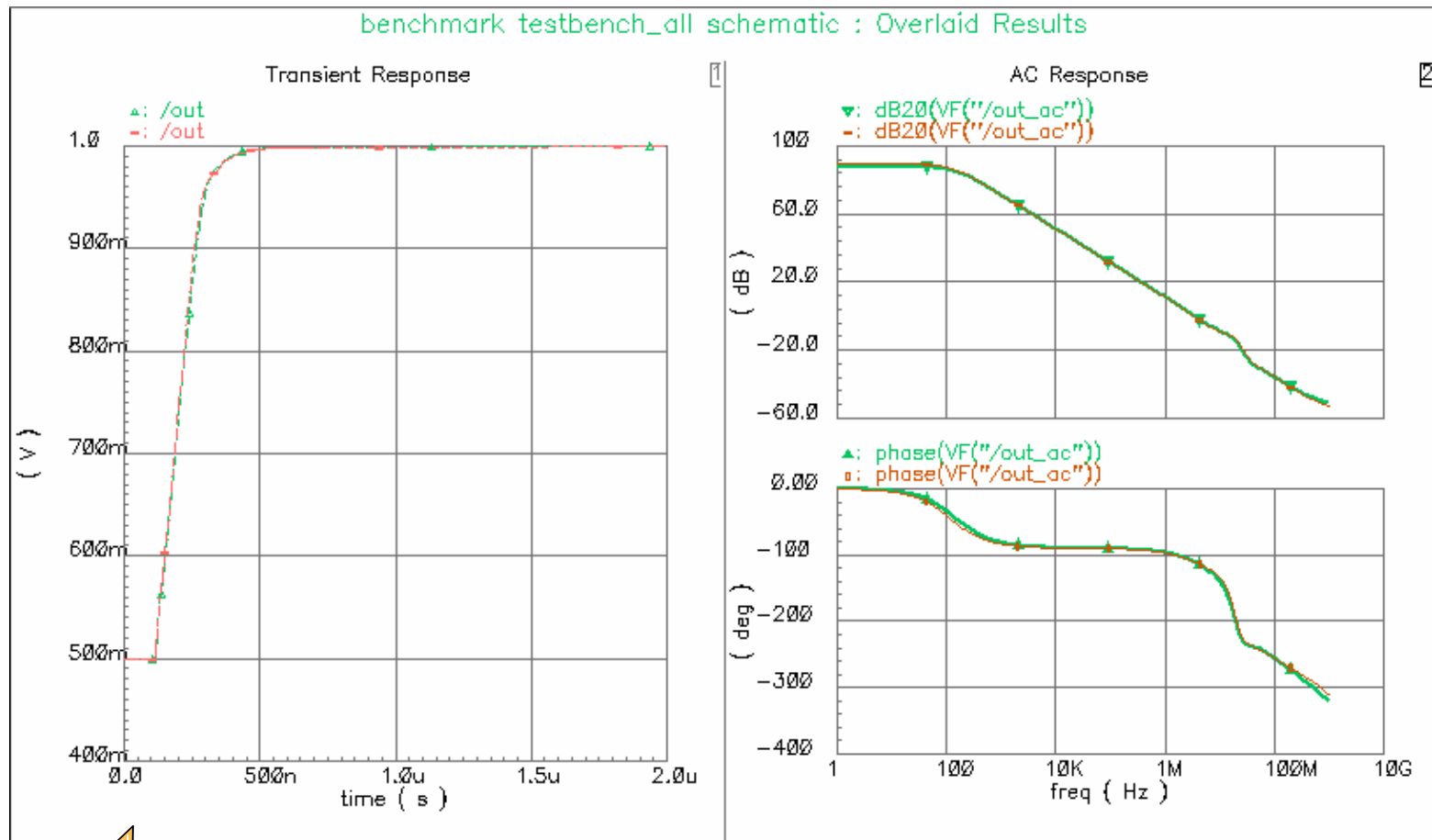
Tolerance Analysis (Node 5)

File Analysis Options

Performance	Bound Type	Specification Value	Analysis	Worst-Case Distance	Yield	
Power	Upper	300 u	→	(5.084)	(100.000)	✓
gain	Lower	80	→	6.690	100.000	✓
ugf	Lower	1 meg	→	(5.261)	(100.000)	✓
phaseMargin	Lower	60	→	(6.473)	(100.000)	✓
gainMargin	Lower	10	→	4.086	99.998	✓
Overshoot	Upper	10 m	→	(5.909)	(100.000)	✓
sR	Lower	500 k	→	4.906	100.000	✓

All analyses finished.

Simulation Results: Nominal vs. Yield Optimized Design

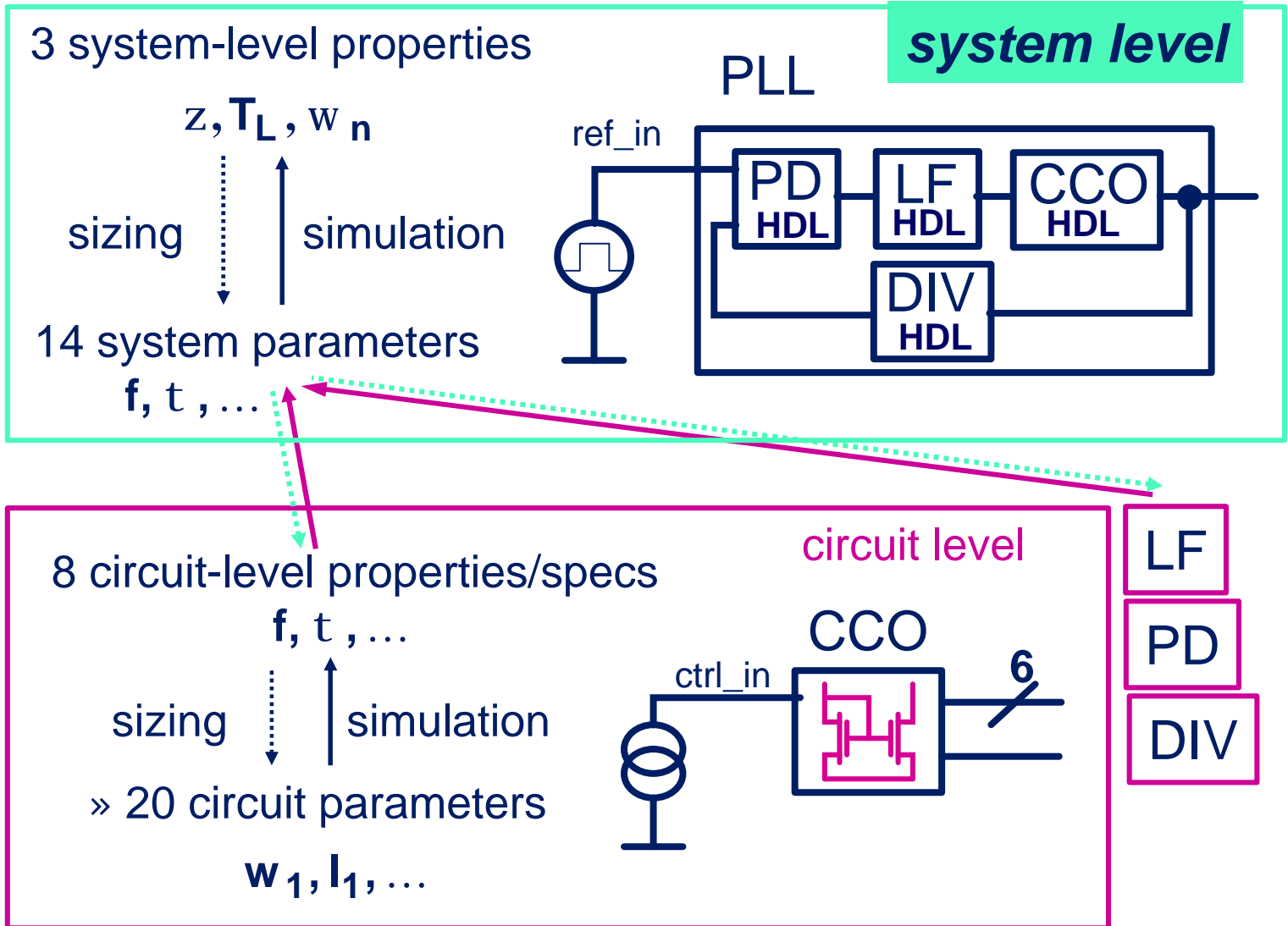


Nearly no deviation in circuit performance, but yield improvement from 96% to 100%

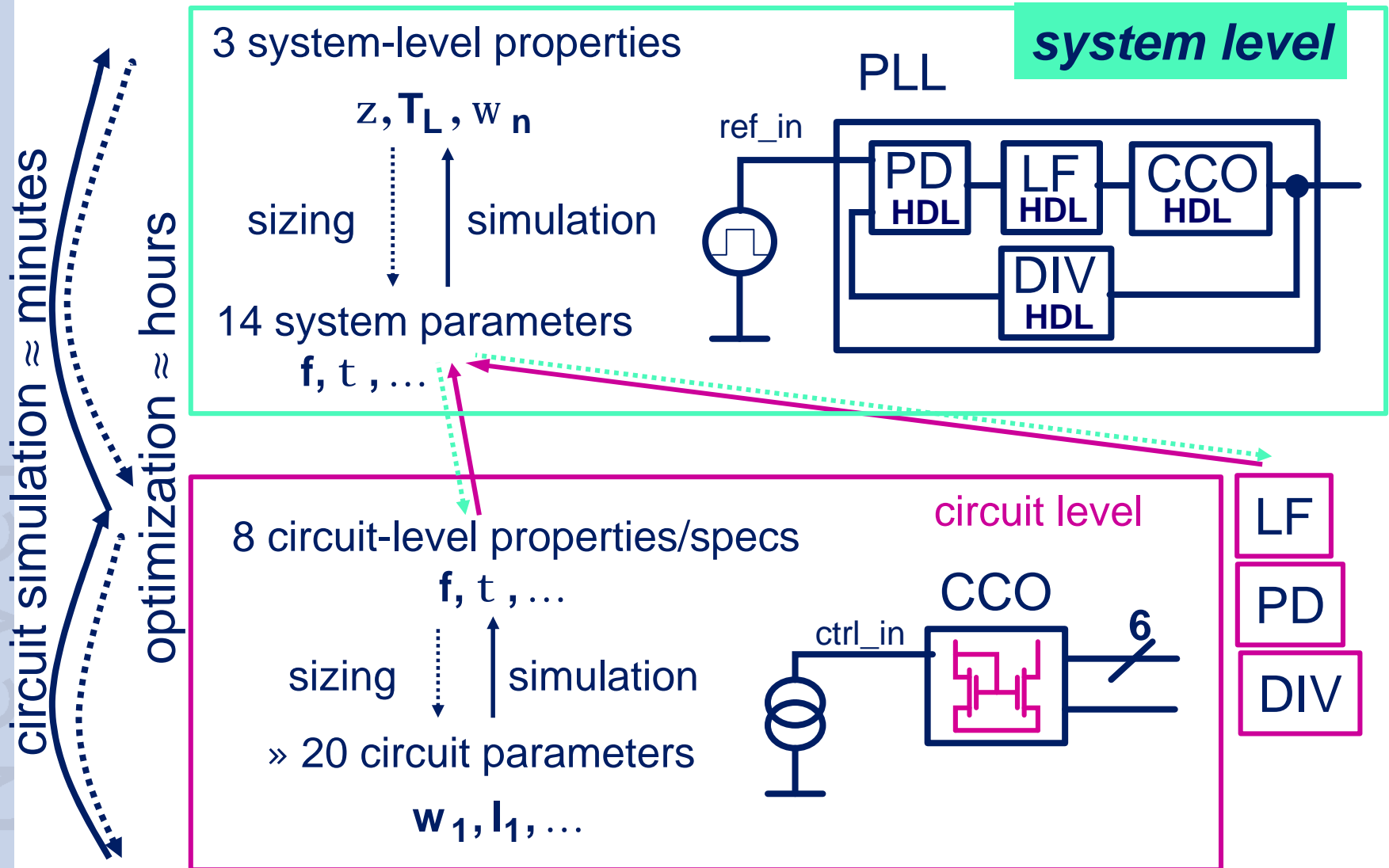
Hierarchical Sizing: Bringing Together ABM and Sizing

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circuit simulation without BM \approx 20h
optimization \approx weeks

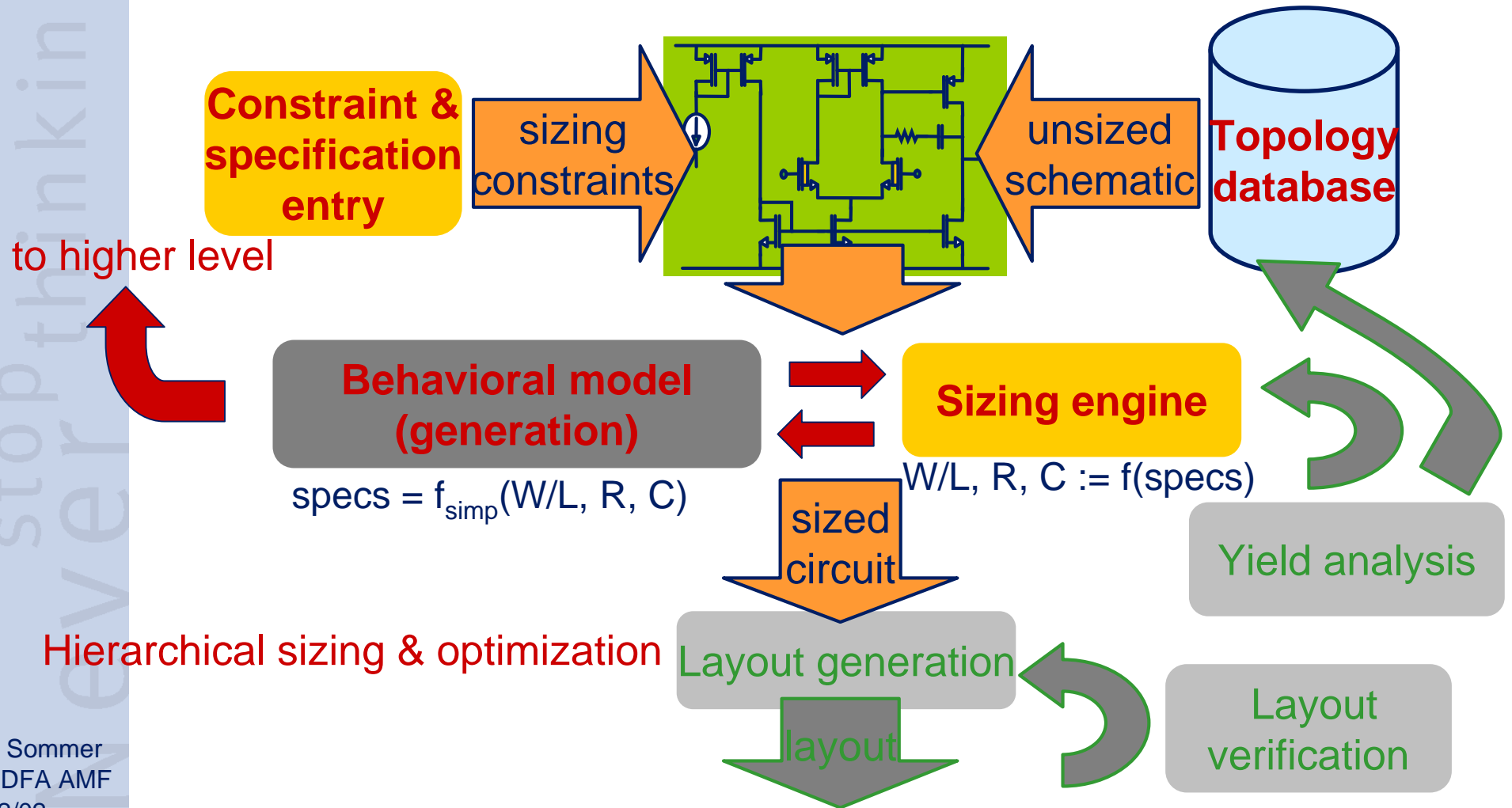


Hierarchical Sizing: Bringing Together ABM and Sizing



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 ever

Reuse-Oriented Hierarchical Analog Design Flow



A Vision: Seamless Flow Integration – Analysis Management Cockpit

stop thinking
ever

