

IP Porting Flow with MunEDA WiCkeD™

IP Porting Flow with MunEDA WiCkeD - User Benefits

- Consistent IP Porting flow of existing design databases between different process technologies
- Makes sizing process for IP porting faster and more efficient
- Can be applied to individual cells or entire libraries
- Improves designers' productivity and convenience
- Efficient re-sizing in the new target technology

IP Porting between Different Processes

The migration of IP & circuits between different process technologies and process design kits (PDKs) can be a very time-consuming, uncomfortable and boring task for a circuit designer.

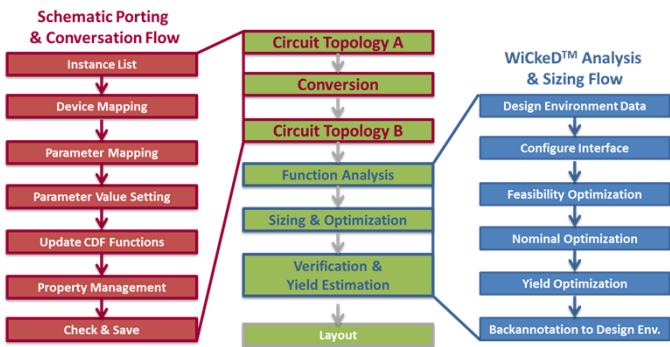
At the beginning of – or during – a new design project, it is often necessary to use and re-use available IP (intellectual property) and circuits from previous projects, instead of designing everything from scratch. Often a new design uses a new or different process technology. Thus, it is necessary to migrate and apply given IP for use with this new target technology. Consequently, circuit designers very often must adapt circuits to the new process by a time-consuming and tedious manual process.

Michael Pronath, MunEDA Vice President Products & Solutions: "IP and Schematic Porting is one of the key topics. MunEDA WiCkeD Tools are the right answer to the challenges in design based on IP Porting and deliver easy-to-handle solutions to be used in IP Porting projects to make designers' life easier and more comfortable. We see a quickly growing demand from our customers to use our solutions for their increasing porting tasks and issues."

Overview – IP Porting, Conversion & Sizing Flow

IP Porting usually follows a structured 2-step design flow. In the first phase the given schematics and topologies will be converted from the source to the target technology. In the second phase these IP will be sized for the new target specifications and optimized for the new target process technology.

IP Porting Design Flow



Picture: Overview - IP Porting, Conversion & Sizing Flow

IP Porting – Types and Challenges

IP porting can be versatile, and it includes different tasks:

- **Horizontal Porting:** Migrating IP from one technology node to the same node of a different foundry due to second sourcing, fab consolidation or foundry migration.
- **Vertical Porting:** Migrating IP from a technology node to a smaller one, usually from the same fab or foundry.

Both are challenging, especially for analog-/mixed-signal designs, RF designs, IP libraries and memory cells because many blocks and even entire SoCs must be migrated in a short time, mostly by a very limited number of designers. Furthermore, there is no simple rule for shrinking AMS/RF, I/O and full-custom digital designs. Every block needs adjustment of geometries, biasing, etc. even if specs don't change. Therefore, it is necessary to migrate and port the schematics individually to conform with technology constraints, or to meet enhanced functionality or performance specifications.

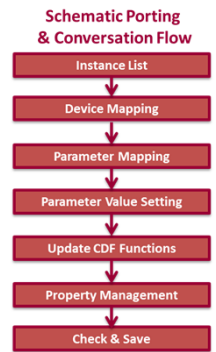
Migrating IP is a challenge because:

- Different device parameters (vth, etc.) require adjustment of biasing and small-signal parameters
- W, L shrinking is desirable, but not as simple as digital
- Some devices (mimcaps, inductors, etc.) may or may not be available, or may be of a quite different type
- Circuit topology may need modification
- Layout shrinking in integrated technologies is insufficient

Step 1 – IP Porting Schematic Conversation - from source to new target process technology

The first of the described two steps of an IP Porting Flow cares for the conversation of given schematics and topologies from the source to the target process technology. Starting with the instance list there is a necessary mapping of device primitives and device parameters including parameter value settings that will be updated with the corresponding CDF functions.

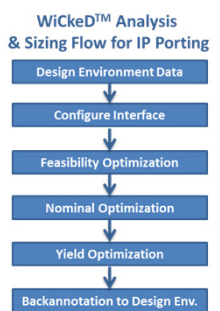
This is followed by the property management like changing of device properties e.g. scaling of devices (e.g. lengths, widths, m-factors). The conversion flow usually works on the schematics of the given schematic entry tool of the used design environment and is supporting design variables and pPar parameters. The symbols must have the same pins to pin location.



Step 2 – IP Porting Analysis & Sizing Flow with WiCkeD

After conversation to the new process design kit (PDK) the flow often requires manual changes by the designer to some features e.g. topology changes by adding new features (power-down, tail-torail operation, cascodes, etc.) or handling limitations (e.g. using low-Vth devices at critical points to reduce minimum supply voltage). At this point, the blocks have an initial sizing which is derived from the sizing of the original design and which (usually) needs optimization to meet the specifications.

The tools from MunEDA WiCkeD can be used to analyze and size the ported topology for new specifications and optimize for the requirements of the target process technology.



Apart from further analysis and diagnosis steps possible with WiCkeD the following steps to size a topology will be usually fulfilled:

1. Simulation & Functional Analysis with industrial standard SPICE simulator from WiCkeD simulation GUI
2. Feasibility Optimization with WiCkeD FEA: checks constraints and ensured saturation conditions
3. Nominal Optimization with WiCkeD DNO: meets performance specifications for nominal & PVT corners
4. Nominal Optimization (WiCkeD DNO): meets performance spec. for worst-case operating corners
5. Yield Optimization with WiCkeD YOP: minimizes the variance of performance parameters



IP Porting with MunEDA Tools – Customer Success

Faraday Technology - IP porting & Analog Synthesis
Automation Platform using WiCkeD™
MUGM MunEDA User Group Meeting 2008



For more info: http://www.muneda.com/User-Group-Meetings_Europe-2008
www.faraday-tech.com

Thomas Hsieh, R&D Associate Vice President, Faraday Technology Corp.:
"MunEDA's WiCkeD showed the capability as an optimization tool in the key role of our IP porting project. The capacity is a general issue for the simulation-based optimization tool. We successfully could demonstrate the circuit optimization process through the comprehensive GUI and script based flow."



ZMDI - Analog IP Porting by Topology
Conversion and Optimization
IP - ESC 2009, Grenoble, France

For more info <http://www.muneda.com/pdf/publications/>

Andreas Bruening, Director Technology Office, ZMD AG, Dresden:
"After testing MunEDA design and yield optimization tool suite WiCkeD in some very successful pilot projects, we chose it for analysis and optimization of analog and mixed-signal circuits and towards increased yield and robustness of our golden IP library."

IP Porting with MunEDA Tools – Technology Support

- WiCkeD™ Tool Suite for automated design analysis, modeling and optimization of IC & IP design
- <http://www.muneda.com/Products>
- For more information and support contact www.muneda.com

