

Analog Circuit Verification Flow with MunEDA WiCkeD™

Benefits of Analog Circuit Verification with WiCkeD

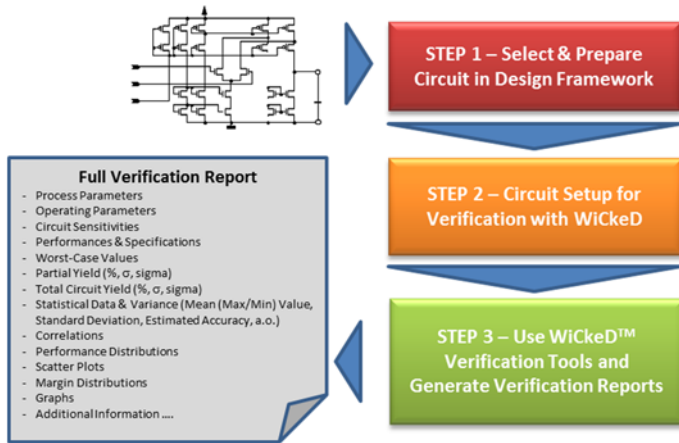
- Increased Design Confidence prior to Tape-out
- Structured Reports for Design Reviews and Management
- Powerful Analog Circuit Verification Tools and Functionalities
- Fully integrated in Standard Design Environments
- Minimum effort required, Easy step-by-step guidance
- Support for ISO 26262 analysis requirements for automotive

Analog Circuit Verification - Motivation

To verify the best functionality and design quality is an essential part of today's analog and mixed-signal circuit design. Circuit designers want to have powerful tools that deliver deep information and insights into circuit behaviour. At the same time these tools should be easy to set up and handle and deliver the required information quickly and comfortably.

Analog Circuit Verification – 3 Steps Flow with WiCkeD

The MunEDA WiCkeD Verification Suite delivers the designer an easy and simple 3-STEPS application flow to verify the circuit designs for the given requirements. Based on the designer's circuit schematics, testbenches and netlists there are only a few simple and easy to do preparation steps in the design framework and in the WiCkeD tool suite itself.



Picture: 3 STEPS - Analog Verification Flow with WiCkeD

WiCkeD Circuit Verification Tools Overview

WiCkeD contains different tools to verify circuit status and quality. Designers can easily check their designs for performance and process sensitivities, worst-case operating corners and partial and total design yield.

WiCkeD Verification Tools	WiCkeD Verification & Analysis Results
	BAS – Basic & Sensitivity Analysis - Sensitivity Analysis & Parameter Sweeps - Process Sensitivities - Parallel Simulation Interface (SPICE, FastSPICE)
	WCO – Worst Case Operation Analysis - Worst Case Operating Corners - Worst Case Performance Values - Circuit Reliability & Robustness Analysis
	MMA – Mismatch Analysis - Local Process variations influence - Mismatch Pair Detection - Analysis of Matching Constraints
	WCA – Worst Case Analysis - Partial & Total Yield Estimation in % and sigma - Consideration of operating conditions and process parameters - Global Process Variation - Local Process Variation (Mismatch) - High-Sigma Variation Analysis
	MCA – Monte Carlo Analysis - Parametric Yield Analysis - Contributor Analysis and Performance Distributions - Scatter Plots - Influence Analysis of Process Variations

WiCkeD Interfaces & Platform Support:

- SUN-Solaris®, Linux, CentOS
- Full Graphical User Interface
- Documented API (C++, Tcl/Tk, Python, etc.)
- Parallel Simulator Interface (LSF, SGE, rsh, ssh)
- Export/Import Interfaces (Matlab, R, SPlus, Verilog-A, VHDL-AMS)

WiCkeD Design Framework & Simulator Support

- WiCkeD SPICE & FastSPICE Simulator and Design-Framework-Interfaces:
 - Cadence® based design environment
 - Mentor Graphics® based design environment
 - Synopsys® based design environment
 - Berkeley Design Automation based design environment
 - In-house Simulators & Environments
- Supporting industrial standard pkg. (Process Design Kit)
- And customized to your environment!

Step 1 – Select & Prepare Circuit in Design Framework

Select in your design framework the circuit toplevel schematic (DUT – Design under test) and prepare the required single or multiple testbenches. Define for the circuit the required performances and extraction statements and expressions with your used extraction language. To check run a simple test simulation to verify the circuit can be simulated. After this preparation simply start WiCkeD from tools section of your design framework.

STEP 1 – Select & Prepare Circuit in Design Framework

- Select Circuit Schematic
- Prepare Single or Multi-Testbench
- Define Circuit Performances
- Define Extraction Statements
- Run Test Simulation

Step 2 – Circuit Setup for Verification with WiCkeD

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- Read Circuit Netlist
 - Assign Operating Parameters
 - Physically identical instances (for multi-testbench setup only)
 - Select Mismatch Parameters
 - Define Performance Specifications

With the WiCkeD Constraint Editor you can automatically read-in the netlist of your selected DUT. Supported by some GUI-steps you assign the operating parameters and define the required operating ranges. In case of multi-testbenches you define also the physically identical instances. Finally you select the mismatch parameters and define the performance specifications for your circuit design.

Step 3 – Use WiCkeD Verification Tools and Generate Verification Reports Automatically

You now can start within WiCkeD history window fully GUI-supported all analysis and verification tools required for your specific verification demand. Based on circuit simulation with your standard SPICE or FastSPICE you verify your circuit

STEP 3 – Use WiCkeD™ Verification Tools and Generate Verification Reports

- Verify Circuit Sensitivities
- Verify Worst-Case Operating Corners
- Verify Global Statistical Variation & Yield
- Verify for High-Sigma and Robustness
- Generate Verification Reports Automatically

for sensitivities, worst-case operating corners, global statistical variation and yield, high-sigma values and robustness, and many influence factors more.

Result: Detailed Verification Reports – Structure & Content

After the described simple steps the designer can easily generate a detailed VERIFICATION REPORT for design review reason containing following information:

- Process Parameters
- Operating Parameters
- Circuit Sensitivities
- Performances & Specifications
- Worst-Case Values
- Partial Yield (% σ)
- Total Circuit Yield (% σ)
- Statistical Data & Variance (e.g. Mean (Max/Min) Value, Standard Deviation, Estimated Accuracy, a.o.)
- Correlations
- Performance Distributions
- Scatter Plots
- Margin Distributions
- Graphs
- and more



Circuit Verification with MunEDA Tools – Solutions that help!



- WiCkeD™ Tool Suite for automated design analysis, porting, verification, modeling and optimization of IC & IP design
- <http://www.muneda.com/Products>
- For more information and support contact www.muneda.com

