

DATASHEET

MunEDA WiCkeD™ Integration to Mentor Graphics Custom IC Design-Flow: Mentor Graphics® IC Station Schematic (DesignArchitect-IC) and Questa ADMS® (Eldo®, EldoRF®, ADiT™, Questa®) Circuit Simulation

WiCkeD Tool Suite

Design for Yield - WiCkeD DFM-DFY Tools Overview

WiCkeD is a comprehensive and powerful software tool suite for analysis, modelling, optimization and verification of analog and mixed-signal circuit designs.



WiCkeD supports the circuit designer with interactive manual, semi- and full-automatic tools to improve and optimize integrated circuits for functionality, performance, robustness, and yield.

Features

WiCkeD includes tools and methodologies for

- Topology Analysis & Constraint Management
- Specification-driven Performance Analysis & Optimization
- Response Surface Modelling
- Yield & Robustness Analysis, Diagnosis, and Optimization

WiCkeD can be operated either through a graphical user interface or a programmable scripting interface (batch mode).

Third Party Support

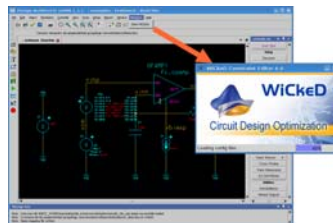
WiCkeD is integrated in and supports the main commercial circuit design environments and simulators including Mentor Graphics®, Synopsys®, Cadence®, and others.

WiCkeD Interface to Mentor Graphics® Custom IC Design-Flow

WiCkeD ideally complements the Mentor Graphics Custom IC Design Flow. This enables circuit designers to access and utilize all WiCkeD tools intuitively from the familiar Mentor-based design environment.

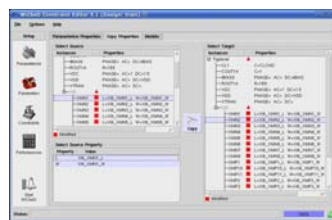
WiCkeD Interface to Mentor Graphics IC Station Schematic – Schematic Editor**

WiCkeD can be started directly from the menu entry in the IC Station Schematic editor with fully automated retrieval of the design data from and back-annotation to schematic & netlist.



Start WiCkeD directly from IC Station Schematic

WiCkeD directly retrieves the design and hierarchy data from the IC-Station or netlist followed by a fully automatic parameterization of schematic and netlist design parameters as well as constraint setup and editing. Specifications for circuit analysis and optimization can be easily entered in the WiCkeD Constraint Editor.



WiCkeD Constraint Editor: Management of Constraints, Parameters, Performances, Specifications

the IC Station Schematic editor. The technology setup (nominal, corner, mismatch, global statistics) will be done automatically from the pdk using a technology based configuration file.

WiCkeD Interface to Mentor Simulation Environment

WiCkeD fully supports Mentor Graphics Questa ADMS circuit simulators including Eldo®, EldoRF®, ADiT™, and Questa® from IC Station Schematic, netlist stand-alone as well as from thirdparty design environments.

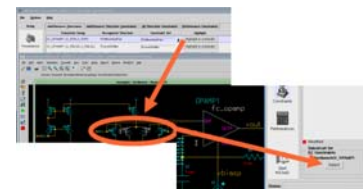


Mentor Graphics IC Design Flow

WiCkeD is fully compatible with Eldo®, EldoRF®, ADiT™, and Questa® Design-for-Yield Process and Interconnect Variation Analysis, supporting Monte-Carlo Analysis and many other features.



WiCkeD simulation environment interface to Mentor Graphics Questa ADMS (Eldo, EldoRF, ADiT, Questa) - based simulation environment



Cross probing between IC Station Schematic schematic and WiCkeD

Parameterized devices, instances and hierarchies can be highlighted from WiCkeD Constraint Editor directly in

***) also DA-IC DesignArchitect-IC

WiCkeD OVERVIEW

Tools to improve circuit design performance and yield

WiCkeD offers several tools for enhanced circuit analysis, modelling, optimization, and verification. These tools enable customers to reduce the design times of their analog and mixed-signal circuits and to maximize robustness, reliability, and yield.



- WiCkeD™ Tools**
- WiCkeD™ Basic - **BAS**
- Circuit Analysis Tools**
- Nominal Diagnosis - **NOD**
- Parameter Screening - **SCG**
- Worst Case Operation - **WCO**
- Monte Carlo Analysis - **MCA**
- Worst Case Analysis - **WCA**
- Worst Case Diagnosis - **WCD**
- Mismatch Analysis - **MMA**
- Circuit Modelling Tools**
- Model Generation - **RSM**
- Circuit Optimization Tools**
- Feasibility Optimization - **FEA**
- Determ. Nominal Optimization - **DNO**
- Global Nominal Optimization - **GNO**
- Yield Optimization - **YOP**
- Interface Tools**
- Scripting Interface - **SCR**
- Simulator / Framework / Interfaces - **SFI**
- Multi-Testbench-Environment - **MTB**

MunEDA WiCkeD Tools Overview

Starting with a basic design history WiCkeD delivers a powerful compilation of features that enable the circuit designer to do enhanced topology analysis, constraint setup and constraint management. Furthermore, it includes different analyses for circuit performance, parameter sensitivities and correlations within a well documented project.

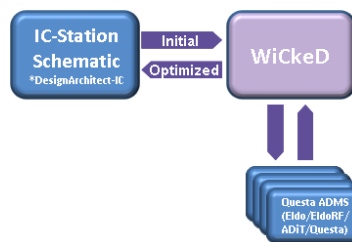
Based on this the advanced WiCkeD tools for circuit analysis, optimization, modelling, and verification can be used by the designer to check and improve the circuit functionality, performance,

robustness and yield in the desired operating environment.

Mentor Graphics based WiCkeD Designflow

Industry-proven design & sizing environment

WiCkeD is seamlessly integrated into Mentor IC-Station Schematic and has a tight interface with Mentor Questa ADMS simulation environment.



Designflow Mentor IC Station Schematic with Questa ADMS & MunEDA WiCkeD

A user of WiCkeD typically performs six steps to analyze and optimize a circuit starting from Mentor Graphics IC Station Schematic & Analog/Mixed-Signal simulation & verification environment:

- STEP 1 – Select DUT in IC Station Schematic Editor
- STEP 2 – Define outputs in IC Station Schematic Editor
- STEP 3 – Start WiCkeD from IC Station menu entry
- STEP 4 – Set parameters, performances (outputs) and constraints in WiCkeD Constraint Editor
- STEP 5 – Analyze, model and optimize your circuit with WiCkeD and verify the results with WiCkeD and Questa ADMS (Eldo, EldoRF, ADiT, Questa)
- STEP 6 – Automatically back-annotate results from WiCkeD to IC Station Schematic and continue with Mentor Graphics layout tools

MunEDA in Mentor Graphics OpenDoor™ Partner Program



MunEDA is member of the Mentor Graphics OpenDoor™ Program since 2005.

APPLICATIONS

- IC performance & yield analysis, modelling, and optimization
- IP porting & reuse
- IP & technology migration
- Supports fab migration & fab light strategies
- Supports transistor-level and system-level circuit design

CUSTOMER BENEFITS

- Reduce design time & effort and improve design quality significantly
- Detect design failures before tape-out and going to fab
- Avoid expensive respins & redesigns, reduce fab-runs
- Achieve high yield and profits

SPECIFICATIONS

WiCkeD Inputs/Outputs

- Mentor Eldo netlist format (direct, socket), ADiT, Questa ADMS
 - Technology Data – PDK process design kit
 - Optimized netlist/schematic
 - Generated behavioural models for system-level optimization
- Platform Support & Features**
- Linux, SUN Solaris®
 - Documented API (Tcl/Tk, Python)
 - Export/Import Interfaces (Matlab, R, SPlus, VerilogA, VHDL-AMS)

SUPPORT & SERVICES

Mentor Graphics

For support of mentioned Mentor Graphics products please contact www.mentor.com.

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